Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 310-311

G-3-1 (Invited)

Challenges to Achieve THz SiGe HBTs

G. Freeman, D. Greenberg, J.-S. Rieh, A. Stricker
IBM Microelectronics, Semiconductor Research and Development Center
2070 Rt. 52, Hopewell Junction, NY 12533
freemang@us.ibm.com 845-892-4690

1. Introduction

Great progress has recently been achieved in SiGe HBT performance, with f_T demonstrations over 350GHz [1][2] and ring oscillator delays below 3.6ps [3]. Although some key material properties of silicon are inferior to those of III-V devices, the ability in silicon to reduce parasitic resistance and capacitance through complex device structures has enabled near performance parity between silicon and III-V devices.

The substantial progress in SiGe HBT performance has come about through both material and structural innovation. The introduction of carbon into the SiGe epitaxy has enabled significantly reduced base widths and process flexibility by reducing the base dopant diffusion during processing. Many structural innovations have also been employed, with the effect of reducing parasitic resistance and capacitance and further reducing base dopant diffusion (e.g., see [3][4]).

Continuing this trend of performance improvement, one may expect SiGe HBTs to soon exceed performance of one THz. Difficulties in achieving performance and reliability for such high performance devices must be overcome. To better understand today's performance limitations, we have performed TCAD simulations. For the purpose of understanding the different issues, we divide the SiGe HBT into two portions. As shown in Figure 1, the device may be divided into the intrinsic and the extrinsic regions. We define the intrinsic portion to include the two-dimensional emitter-base junction and to contain about 80% of the spreading current flow into the collector. We first consider the intrinsic performance challenges, and then the extrinsic challenges. Following this, we discuss the more practical challenge of reliable operation in THz SiGe HBT devices.

2. Intrinsic device performance

Intrinsic device performance continues to be dominated by transit time, and as a result, the device vertical dimensions and carrier velocity remain key performance limiting factors. Despite the material advances providing reduced diffusion in recent years, the diffusion of the base dopant still is a key factor determining vertical device dimensions. This is in part a result of the complex device construction in today's SiGe HBT. High-temperature anneals (i.e. 900-1000^{o}C) for emitter drive-in and silicides promote diffusion and complex structures require diffusion (i.e. to reduce resistance or neutralize edge defects). New materials, new structures, and new processes will inevitably improve the vertical dimensions.

With these ever-reduced dimensions, the carrier velocity (now dominated by phonon and impurity scattering) will start to enjoy benefits of ballistic transport. Structural elements, such as a designed-in conduction band discontinuity at the emitter-side of the neutral base, should provide increased performance advantages.

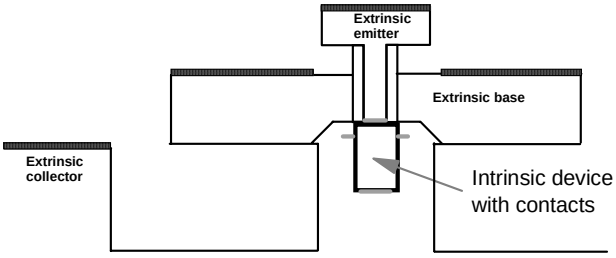

Figure 1: SiGe HBT intrinsic and remaining extrinsic portions.

Further, collector doping increase will push device operation to ever-higher Kirk-effect currents. This improves device f_T through the well-known proportionality to I_C and thus g_M. This also reduces space-charge dimensions and thus transit time. The tradeoff of performance compared to increased capacitance is generally favorable to f_T improvements and less favorable to f_{MAX} improvements.

Through TCAD simulations, we have explored intrinsic device performance exceeding f_T=1 THz. The work is similar to the drift-diffusion simulations reported in [5], except with full 2D process simulation and 2D device operation including self-heating effects. Device simulations were performed on an intrinsic region indicated by the rectangle of Figure 1, including low electrical and thermal resistance connections in locations shown by the gray shapes outside the base, emitter, and collector. The process and device simulation was first calibrated to the 350GHz device reported in [1]. The THz intrinsic device compares to the 350GHz device with 3X higher peak f_T current density J_C, 3X higher collector-base capacitance C_{CB}, and 1/3 the collector resistance R_C.

3. Extrinsic performance

The extrinsic device, while often neglected in analysis of performance improvements, truly has a significant effect on performance, yet also provides the greatest opportunity because there are limited fundamental tradeoffs. To illustrate, consider Figure 2, which shows normalized R_B and C_{CB} values versus f_T across many reported devices [3,4,6,7,8,9,10,11]. Note that while it is important to reduce C_{CB} and R_B for performance improvements, because C_{CB} is largely an intrinsic-dominated parasitic, and R_B is largely an extrinsic-dominated parasitic, the advances in technology have found

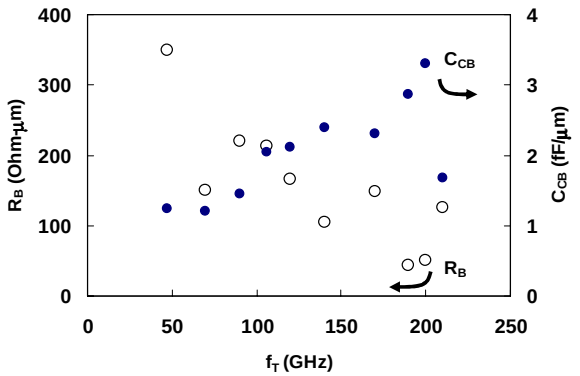

Figure 2. Base resistance R_B (open symbols) and collector-base capacitance C_{CB} (solid symbols) for reported SiGe HBTs. Values are normalized to emitter length [3,4,6-11].

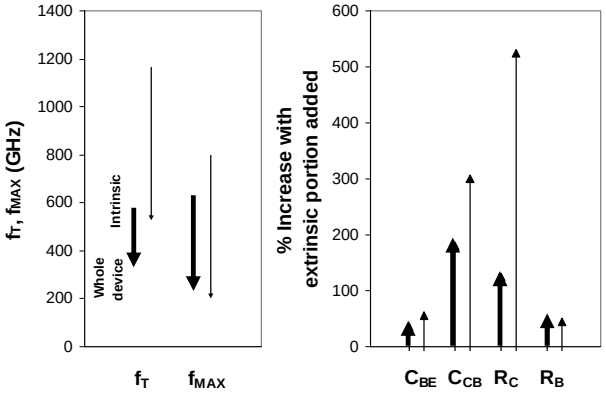

Figure 3. Electrical parameter shifts with addition of the device extrinsic portion as predicted by TCAD simulation. Thick arrows are the 350GHz device as reported in (14); Thinner arrows are simulated 1.16 THz (intrinsic) device.

limited opportunity in C_{CB} reduction, but much greater R_B opportunity shown by the reduction in R_B with increasing f_T.

To estimate the performance limiting effect of the extrinsic device, consider the comparison of device f_T and f_{MAX} performance for both the 350GHz (extrinsic) device and the THz (intrinsic) device, as shown in Figure 3. In this comparison, we have added essentially the same extrinsic device structure to the two intrinsic devices. The exception is that the extrinsic portion of the THz device has reduced epitaxy thickness above the subcollector, and this increases extrinsic C_{CB}. For the 350GHz (extrinsic) device, f_T=557 and f_{MAX}=630 GHz intrinsic performance become 332 and 224 GHz with the addition of the extrinsic device respectively. The latter correspond approximately to measured values reported in [1]. On the THz (intrinsic) device, f_T=1165 and f_{MAX}=798 GHz intrinsic performance become 525 and 171 with the extrinsic device added respectively.

With the higher intrinsic performance, the device is more sensitive to the parasitic resistance and capacitance. This is a result of the need to reduce all the parasitic and transit times commensurately. With the reduction in the intrinsic portions of delay, the extrinsic portions become more significant. Figure 3 also shows that the C_{CB} and R_C are especially affected by adding the extrinsic device.

4. Practical effects

Increasing collector doping, a necessary part of achieving higher performance, results in both higher electric fields and higher operating current densities. These effects result in a lower breakdown voltage and higher device self-heating. While not imposing hard limits to device performance, they must be carefully considered in device design and reliability assessment, becoming more difficult in THz devices.

Avalanche current has been shown to induce base current degradation at low biases due to the hot-carrier damage in the emitter-base junction edge dielectric [12]. Yet, as shown so far in 200GHz SiGe HBTs, these effects do not limit the device bias to below BV_{CEO}, and the effects are expected to have minimal impact to most applications.

Device self-heating, on the other hand, imposes a more serious limitation and both the device and circuit designer need to be aware. Unlike in CMOS devices, which have exhibited linear currents in the range of 700-1000µA/µm, with recent maximum voltages in the range of 1V, the SiGe HBTs with f_T>100 GHz have called for currents in the range of 1500 µA/µm achieved at voltages in the range of 1.5V. The result is greater device self-heating that needs to be managed by the device designer by reducing emitter stripe width and other layout optimization techniques, and by the circuit designer through careful analysis of device temperature impact on metal reliability.

5. Conclusions

There remains significant opportunity for SiGe HBT performance improvement. Many processes available in CMOS have not yet been implemented in SiGe HBTs: spike anneals, low barrier silicides, and self-alignment techniques are to name a few. Continued vertical scaling on the intrinsic device will hinge on new processes and materials. The extrinsic device will be the most challenging to continue parasitic resistance and capacitance reduction.

6. References

[1] J.-S. Rieh et. al., Proceedings IEDM 2002, pp 771- 774
[2] J.-S. Rieh et. Al., Proceedings IPRM, 2003 pp 374 -377
[3] H Rücker, Proceedings IEDM, 2003, pp 121-124
[4] B Jagannathan, et. al., IEEE EDL 23:258-260 May 2002
[5] Y Shi, G. Niu, to be published Proc. BCTM 2004
[6] G Freeman, et. al. Proceedings ESSDERC, Leuven, 1999,
[7] A Joseph, Proceedings of the 2001 BCTM, pp. 143 -146
[8] J Bock, Proceedings IEDM, 2001, pp 344-347
[9] K Washio, et. al. Proceedings IEDM, 1999, pp 557-560
[10] P Deixler. Proceedings BCTM 2002, pp. 201-204
[11] S Wada et. al., Proceedings BCTM 2002, pp. 84-87
[12] Z.Yang et. al., Proceedings IRPS 2003, pp. 339-343