Evaluating and Designing the Optimal 2D Collector Profile for a 300 GHz SiGe HBT

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Abstract
TCAD simulations allowed to gain insight into a 300 GHz HBTs current distribution. Design guidlines for the optimal mask width of a selectively implanted collector (SIC) doping profile could be derived.

1. Introduction

High speed applications operating above 50 GHz require transistors with transit frequencies (f_t) higher than 200 GHz. To reduce costs a monolithic integration with a mixed signal CMOS part is favorable. This initiated the introduction of SiGe hetero junction bipolar transistors (HBT) [1] combined with CMOS ULSI logic.

To achieve high switching speeds it is not sufficient to reduce the HBT's dimensions, the transistors parasitics like the base resistance (R_b) or the collector-base capacitance (C_{cb}) must be minimized too [2]. More important, however, is the design of the SIC doping profile, which has a strong impact on the carrier transit time through the transistors base, collector, and intermediate depletion zone [3]. Therefore the collector profile is usually a trade-off between speed (f_t), C_{cb}, break down voltage (BV_{ceo}), and unity power gain (f_{max}).

$$f_{max} \cong \sqrt{\frac{f_t}{8\pi R_b C_{cb}}} \quad (1)$$

According to equation (1) a reduction of C_{cb}, with constant R_b and f_t would lead to an increase of f_{max}. But in a high speed HBT f_t is a complex function of the 2 dimensional carrier path through the base-collector-depletion and intrinsic collector-zone, and therefore the assumption 'f_t=constant' does not hold anymore. Using TCAD, it is possible to model this complex behavior of the HBT [4] and optimize the 2D doping profile for best AC performance.

2. Impact of the 2D SIC doping profile on transistor speed

Figure 1 shows a schematic cross-section of an advanced SiGe HBT. The SIC is placed between an intrinsic epitaxial layer (Epi) and the low temperature epitaxy (LTE) which contains the base layer and the graded Ge profile. To reduce the collector capacitance the active area of such a transistor may be surrounded by a shallow trench isolation (STI).
To verify and calibrate the implanted collector profile we compared the simulation results depicted in Figure 2 with 1D SIMS profiles as well as to a cross section of the device. To highlight the 2D doping profile we applied a n-dopant sensitive etch revealing the base collector junction. A 2D overlay of the highlighted SEM picture with the simulation profile matched within measurement accuracy. In both cases the lateral diffusion length is approximately 80% of the vertical diffusion depth. A method for the optimization of the vertical profile has been presented at ISTDM2003 [5].
The width of the neutral base or collector depletion zone (DZ) affects both, the collector-base-capacitance (C_{cb}) as well as the carrier transit time through it. While C_{cb} increases with a narrower depletion zone, the transit time gets shorter.

$$DeplCont = \log_{10} \frac{n + p}{|n_d - n_a|} \quad (2)$$

Using equation (2), where n and p are the carrier and n_d and n_a the donor and acceptor concentrations, 2D depletion contours have been calculated for different SIC mask openings (Fig. 3 and 4) with the transistor biased at V_{be}=0.7V and V_{cb}=0.5V. While both depletion levels are comparable under the emitter (-4), the shape of the depletion zone with the narrower SIC mask features a 22% lower C_{cb}. This is due to its larger width close to the edge of the silicon while still providing a short path in the center for the majority of the carriers. Simulating the current flow lines reveals that 80% of the HBT's total current flows within 23% of the silicon width (Fig. 5). Therefore a narrow selectively implanted collector profile creating a triangular depletion zone is favorable as long as it does not pinch the current flow. A "waist" in the flow lines (Fig. 5) increases the collector resistance R_c and in consequence τ R_cC_{cb} resulting is a f_t loss. Thus the ideal current flow is as vertical as possible to minimize the transit time through the depletion zone. Figure 6 summarizes the trends for f_t, f_{max}, I_c at peak f_t, and C_{cb} for various SIC mask openings (100% = full silicon width; 0% = no SIC). As expected f_t runs through a maximum at 20% silicon width, I_c gets pinched and rolls off when the SIC is too point like, C_{cb} decreases with an enlarging depletion zone, and f_{max} increases due to the reduction of C_{cb} and partially increasing f_t.

3. Conclusions

The SIC profile in a SiGe HBT must be tailored to the width of the major current flow. A profile that is too narrow pinches the current and thus reduces f_t through an increased τ R_cC_{cb}. A profile that is too wide increases the average carrier path through the depletion zone and adds unnecessary C_{cb}, which again increases the R_cC_{cb} time constant as well as reduces f_{max} (Equation 1). Through TCAD it was possible to understand the device's physics and, based on this, find the optimal width for the selectively implanted collector profile for a given transistor layout.

References

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Acknowledgements

We would like to acknowledge John Petrus for finding the time and patience to determine the optimum etch chemistry and application to prepare the sample for the highlighted SEM cross section.

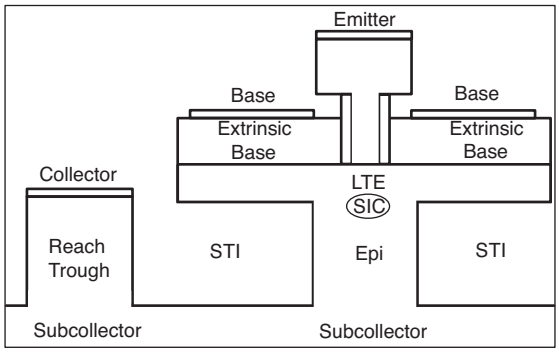

Fig. 1: Schematic cross section through an advanced SiGe HBT. The masked selectively implanted collector is located below the LTE between the STI.

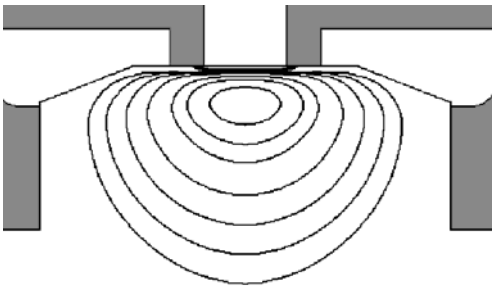

Fig. 2: 2D contour lines of the SIC doping profile calibrated to a SEM cross section with highlighted n-doping through an etch. The lateral diffusion is approximately 80% of the vertical expansion.

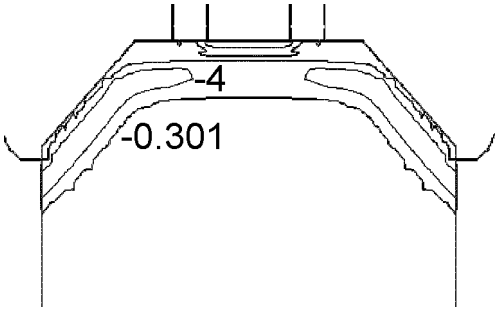

Fig. 3: Depletion contour lines according to equation (2). The width of the DZ is almost independent of the position in the silicon.

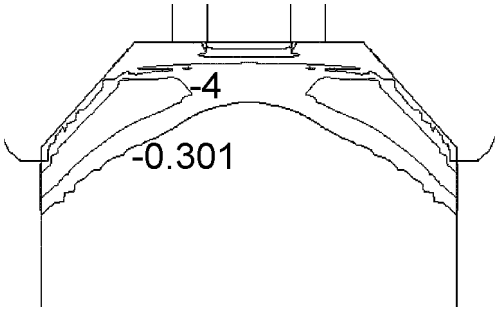

Fig. 4: Depletion contour lines according to equation (2). The side portions of the DZ are extended resulting in a lower C_{cb}.

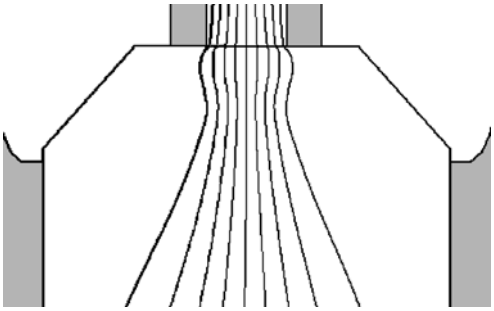

Fig. 5: Current flow lines through a too narrow SIC: the current is pinched which increases R_c and thus negatively influences f_t.

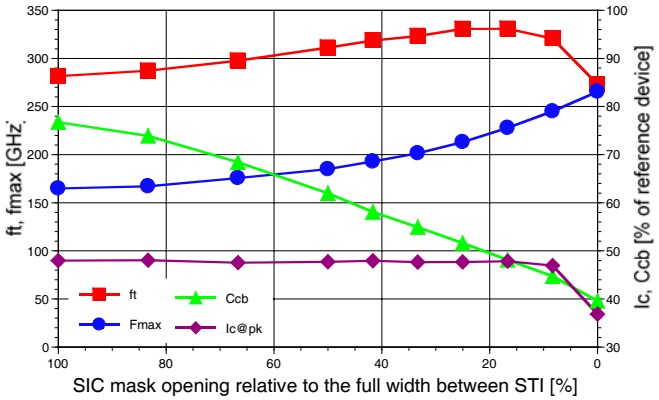

Fig. 6: AC parameters versus SIC mask opening. An optimum was found at about 20% of the total silicon width.