Circuit Design Considerations for Using 100-200 GHz SiGe HBT BICMOS Technology in High-Speed Network ICs

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INTRODUCTION

This paper deals specifically with performance, operating voltage, reliability and integration considerations for using 100-200 GHz SiGe HBTs in high-speed (10-40 Gb/s) network ICs, an application space previously only addressed by InP technology. All indications are that SiGe will be very successful at addressing this new application space, and all facets of the networking IC market.

The SiGe HBT has proven to be a cheaper, viable replacements for GaAs in many different network IC applications. Many 10-20 Gb/s SONET and Ethernet chips have been fabricated. With SiGe HBT now achieving performance over 100 GHz, it becomes a viable replacement for InP-based technologies in the 40-50Gb/s (OC-768) application space, and low-power 10Gb/s operation.

PERFORMANCE AND INTEGRATION

Our first HBT BICMOS technology had a 100 nm base width, and very low average germanium content. This was a "pseudo HBT" - the HBT effect at the E-B junction is incidental, the main purpose is to grade the base to improve the transit time (Fig. 1)[1]. Scaling was achieved by decreasing the base-width with low total Ge dose (to keep total strain low). The effect of vertical and horizontal scaling is shown in Fig. 2. Our current production HBT technology has 120 GHz f_T. We have recently achieved an f_T of 180 GHz, which is a record for SiGe HBTs. The value of 170 GHz at 1 mA, is better than recently reported InP results[2].

Integration is the principle driving force to implement solutions in SiGe BICMOS. All essential devices are available on-chip (Table 1)[3]. The CMOS allows a large amount of (digital) signal processing to be done at low-power and low-cost, at speeds upto 10GHz, without requiring high-power I/O drivers to get on and off a second chip. In the case of critical elements such as resistors and capacitors, the parasitic elements are reduced by placing them a distance from the substrate, between the metal wiring levels. Deep and shallow trench technology is used for capacitance reduction and device isolation (Fig. 3). A new 4μm thick metalliza- tion scheme using aluminum and copper has been developed to provide low-loss transmission lines.

OPERATING VOLTAGE CONSIDERATIONS

There has been much discussion of operating voltage limitations for SiGe, particularly the Johnson limit. We believe that the Johnson limit is wrong and outmoded, and has little relevance to high-speed IC design[4]. Avalanche current exiting the base in most situations passes through a sufficiently low impedance that the device operation extends well above BV_{CEO} (Fig. 4). Our measure- ments show that for Rs<50Kohm, the breakdown voltage $BV_{CER} = BV_{CBO} >> BV_{CEO}$. The 6-7V BV_{CBO} thus ensures that conventional supply voltages in these ICs can be safely supported provided the reverse base current is accounted for. Low-voltage (3-4V) electro-optic modulators would be required for using SiGe in the modulator driver circuit.

YIELD AND RELIABILITY

Based on prior SiGe technologies achieving good yields with upto 80,000 HBTs, we expect the integration level to exceed 10,000 HBTs for 100+ GHz SiGe, resulting in chip-count and power reductions. High-temperature stress results on our 90 GHz technology (Fig. 5) show very little device degradation (typically <8% β degradation), with no catastrophic fails. The current density is high, but because of the small emitter width (large by silicon standards!) the total current can be easily carried by the copper metallization. In addition, thermal measurements show a reasonable 30-40^oC temper- ature rise ($T_{AMBIENT}$=105^oC, T_J=135-145^oC), similar to that in III-Vs. Note that typical SiGe processing temperatures (including contact formation) of 750-950^oC are *several hundred ^oC* above III-V process- ing temperatures and dopant diffusion

coefficients (which might be associated with catastrophic failure modes) are at least TEN orders of magnitude lower in Si than in III-Vs! The tungsten stud and Cu metal also contribute to high reliability of the technology.

In conclusion, 100+ GHz SiGe technology shows great promise of addressing the 40 Gbit/s (and higher) and low-power 10 Gbit/s application space. We would like to acknowledge Burlington and ASTC fabs and modelling & reliability groups for their efforts. Parts of this work were supported by

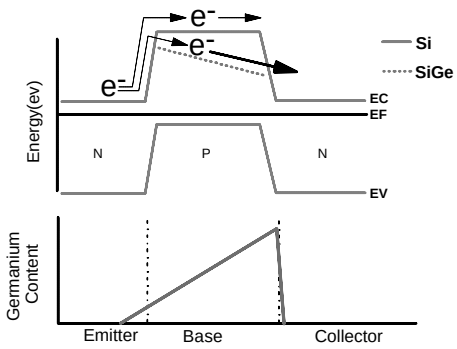

Figure 1. Band diagram and Ge ramp profile of hig performance SiGe NPN HBT

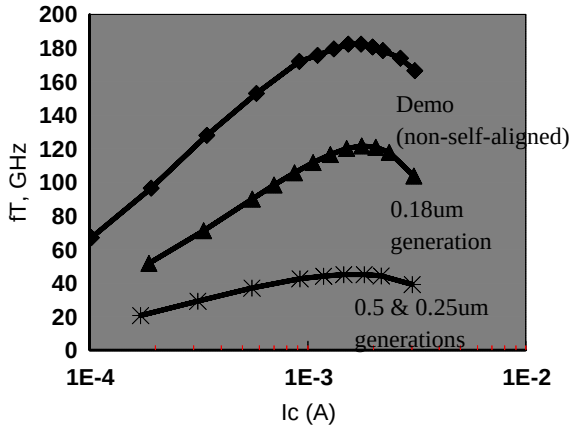

Figure 2: f_T characteristics on different generations of HBT. Each is 2X minimum technology device size illustrating constant current scaling. V_{CB} = 1V.

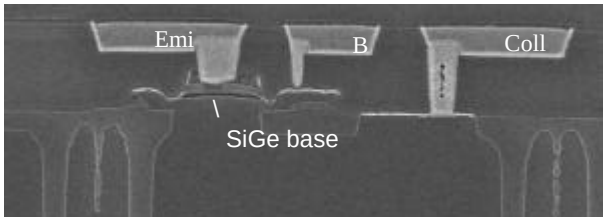

Figure 3: SEM cross-section of 0.18µm, 120 GHz HB Note deep & shallow trench isolation, salicide & copper metal.

FETs	Leff (um)	Idsat (uA/um)
1.8V NFET	0.11	600
1.8V PFET	0.14	260
3.3V NFET	0.29	550
3.3V PFET	0.29	240
Resistors	**Rs (O/Sq)**	**TCR (ppm/C)**
Subcollector	8.1	1430
N+ Diffusion	72	1910
P+ Diffusion	105	1430
P+ Polysilcon	270	50
P Polysilicon	1600	-1178
TaN	135	-750
Capacitors	**Cp (fF/um2)**	**VCR (+5/-5 ppm/V)**
MIM	1	<45
MOS	2.6	5
Inductor	**L (nH)**	**Max Q at 5 GHz**
Al - Spiral Inductor	>=0.7	21
Varactor	**Tuning Range**	**Q @0.5 GHz**
CB Junction	1.64:1	90
MOS Accumulation	3.1:1	300

Table 1. FET and passives available on-chip fo 120GHz, 0.18µm process

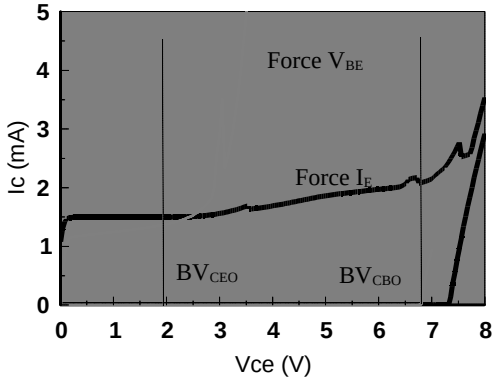

Figure 4. Forced V_{BE} and forced I_E outpu characteristics for 0.18µm, 120 GHz device. Devi area A_E = 0.2x6.4µm^2.

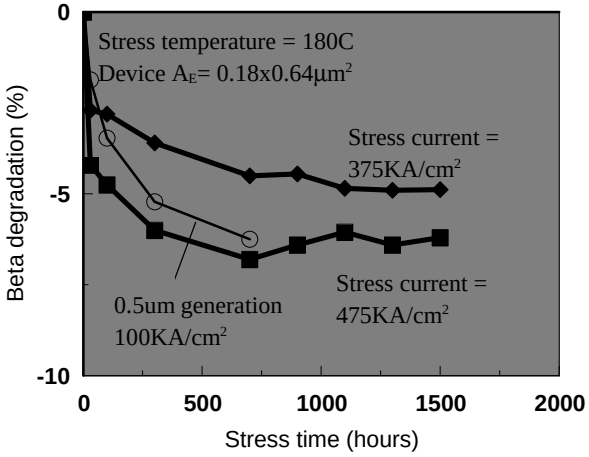

Figure 5: HBT beta degradation vs. time, stressed up to and measured at peak f_T current density for our 0.18µm 120 GHz technology (V_{CE}=3V). Comparison with 0.4µ 50GHz technology at 100kA/cm^2 shown.

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