Foundation of rf CMOS and SiGe BiCMOS technologies

J. S. Dunn
D. C. Ahlgren
D. D. Coolbaugh
N. B. Feilchenfeld
G. Freeman
D. R. Greenberg
R. A. Groves
F. J. Guarín
Y. Hammad
A. J. Joseph
L. D. Lanzerotti
S. A. St.Onge
B. A. Orner
J.-S. Rieh
K. J. Stein
S. H. Voldman
P.-C. Wang
M. J. Zierak
S. Subbanna
D. L. Harame
D. A. Herman, Jr.
B. S. Meyerson

This paper provides a detailed description of the IBM SiGe BiCMOS and rf CMOS technologies. The technologies provide high-performance SiGe heterojunction bipolar transistors (HBTs) combined with advanced CMOS technology and a variety of passive devices critical for realizing an integrated mixed-signal system-on-a-chip (SoC). The paper reviews the process development and integration methodology, presents the device characteristics, and shows how the development and device selection were geared toward usage in mixed-signal IC development.

1. Introduction

Silicon–germanium (SiGe) BiCMOS technology, which achieved its first manufacturing qualification in 1996, is now in its fourth lithographic generation of development. This class of technology integrates high-performance heterojunction bipolar transistors (HBTs) with state-of-the-art CMOS technology. Key technology characteristics for the four generations have been reported by IBM [1–4]. All generations of BiCMOS technology are compatible with an associated IBM CMOS technology in devices, metallization (interconnects), and ASIC design system. **Figure 1** is a SiGe BiCMOS chart showing the evolution of performance and minimum lithographic feature size together with some derivative technologies. As shown in **Figure 2**, the HBT cutoff frequency f_T has improved from 47 GHz in the 0.5-μm generation to 210 GHz in the 0.13-μm generation. The pace of development continues unabated, and there are no apparent barriers to scaling the SiGe HBTs beyond 210 GHz.

The SiGe HBT performance has been significantly improved by a combination of vertical and lateral scaling. Structural improvements included shrinking the emitter width and reducing layer thicknesses for the first three generations and migrating to a new raised extrinsic base (RXB) structure for the 0.13-μm generation. Vertical profile scaling included increasing the drift field by increasing the Ge concentration and reducing the graded base width, adding carbon (C) to decrease diffusion, reducing the thickness of the collector epitaxial layer, and minimizing the emitter thermal cycle. In the 0.13-μm generation, vertical and lateral profile scaling has led to a reduction in the parasitics of the HBT, especially in the base, collector, and emitter resistances (R_B, R_C, R_E) and total collector–base capacitance (C_{CB}). Coupled with the increased f_T, this reduction in parasitics is expected to lead to an increased f_{max} (the maximum frequency of oscillation of a device, often referred to as U, for unilateral matched power gain, or MAG, for maximum available gain) in the devices. All devices in the production technologies must pass stringent quality and reliability tests [5]. Both the 120-GHz and 210-GHz technologies exhibit collector–emitter breakdown voltage with base open circuit (BV_{CEO}) values around 2 V, but this is not a serious concern, because in typical circuits the base is biased through a finite resistance and the true HBT breakdown voltage is between BV_{CER} and BV_{CES} (typically between 3.5 V and 6.5 V. It is more important to know the safe operation area and how large signal parameters vary as a function of use condition [6, 7].

In contrast to the trickle of early circuits [8], there is now a flood of new SiGe products in almost every wired and wireless application area. A sample of the wide

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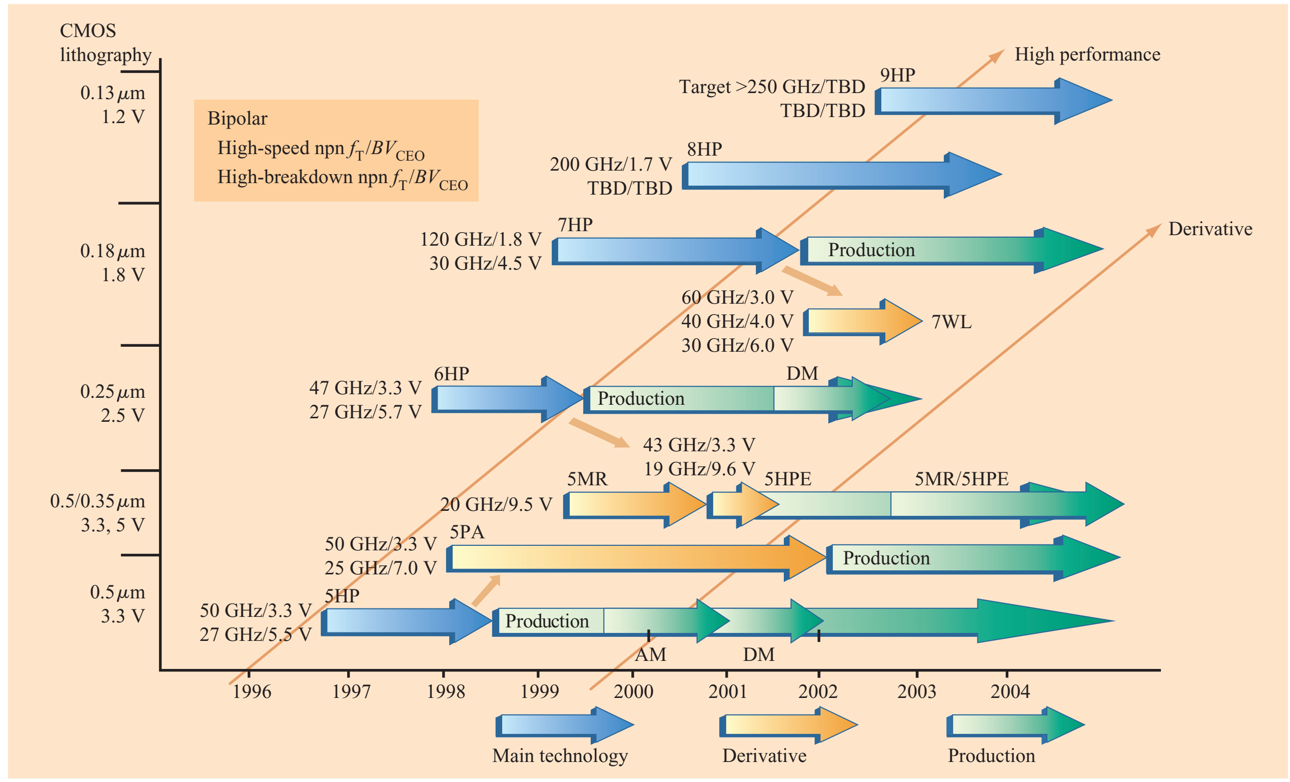

Figure 1

Summary of SiGe BiCMOS and rf CMOS technology.

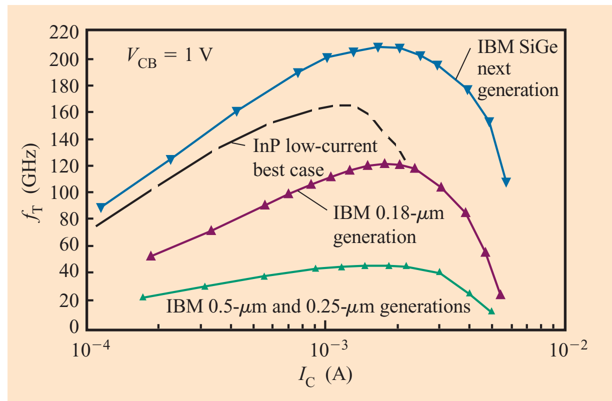

Figure 2

Cutoff frequency f_T vs. I_C for four lithographic generations of SiGe. The InP curve shows recent production InP results.

variety of SiGe BiCMOS circuits illustrates the wide-ranging applicability of these technologies (**Table 1**).

An important aspect of any SiGe BiCMOS technology is the yieldable HBT device count. There are now products with HBT device counts greater than 100000. A good example is a 68 × 69-cross-point switch[1] which contains more than 100000 SiGe HBTs. The largest chip to date is a 10.8 × 10.8-mm OC-48c SONET/SDH mapper with integrated serializer/deserializer integrated clock recovery (CDR) and clock synthesis (CSU).[2] This highly integrated mixed-signal circuit includes 6000 HBTs and 1.2 million CMOS transistors.

The 0.5-μm and 0.25-μm SiGe BiCMOS technologies are ideal for many wireless applications. Areas of analog sections do not scale with decreasing lithography, which reduces the incentive to migrate toward more advanced lithography ground rules [3]. Consequently, a full suite of passive devices is required for any highly integrated mixed-signal chip. The focus in resistors is to achieve good tolerance [~10% on polysilicon (poly) and single-crystal silicon] and reduced parasitic capacitance. For the most stringent requirements, back-end-of-line (BEOL[3]) thin-film

[1] AMCC S2090 preliminary data sheet, Applied Micro Circuits Corporation, 6290 Sequence Drive, San Diego, CA 92121.
[2] AMCC S4803 preliminary data sheet.
[3] Those silicon chip process steps which occur beyond silicon device formation levels (e.g., metal interconnects and interlevel dielectrics).

Table 1 Circuits demonstrated using IBM SiGe technologies, showing their wide-ranging applicability and utility.

Application/Circuit	*Comments*	*Figure of merit*	*Reference*
Model-hardware correlation			
Ring oscillators	ECL differential, typically 250–300-mV swing	5HP–16 ps 7HP – 9 ps, 8HP – 4.2 ps	[8], Nortel (7HP, 8HP), unpublished
Storage			
PRML read channel	Highly integrated BiCMOS design	>75 MB/s (600 Mb/s), product	[2], IBM
RF/WLAN (2–2.5 GHz)			
Integrated VCO	0.5-μm SiGe, tuning using MOS cap	2.5 V, −95 dB_c/Hz at 25 kHz, 9-mA core	[9], IBM
TDMA power amplifier	IS-54-compliant at 800 MHz		[10], IBM
CDMA power amplifier	IS-95-compliant at 1800 or 1900 MHz		[10], IBM
Wireless LAN chip set	Three SiGe chips and one CMOS chip to replace eight GaAs chips	Commercial production part in PCM-CIA cards	[11], Intersil
Wireless down-converter	1-V design, integrated transformer coupling and feedback	Mixer 2.5 mA, LNA 2.5 mA at 1 V, LNA 10.5-dB gain, 0.9-dB noise figure	[8], Nortel
2.5-GHz frequency synthesizer	Three bipolar, four CMOS blocks (200 HBTs, 2500 FETs, ~150 passives)	−91 dB_c/Hz at 100-kHz offset, 2375–2550 MHz, 1-MHz spacing, 44 mW core	[12], IBM
GPS chip set	SiGe 0.5-μm BiCMOS	Direct-conversion front end	[13], IBM and SMI
Microwave/WLAN (5+ GHz)			
Integrated VCO	Fully integrated L, C, varactor tank	To 26 GHz, 3 V, 22-mW core power, 3.6% tune, 84 dB_c/Hz at 100-kHz offset	[14], IBM
Frequency divider	1.9-V, 0.5-μm SiGe BiCMOS	1.9 V, 220 μA, 2.3–5.9 GHz	[8], Nortel
K-band static frequency divider	1/128, inductively peaked input buffer, 0.5-μm SiGe	23-GHz operation demonstrated	[15], HRL
Base station			
Digital, DAC chips	8-GHz clock, highly integrated	−140 dB_c/Hz dynamic range	[16], Siemens
Networking			
Integrated VCO–40G	0.18-μm SiGe, fully integrated	To 25 GHz, digital coarse tuning with MOS capacitors	[17], IBM
Broadband amplifier	0.5-μm SiGe BiCMOS design	9-dB gain, 22-GHz BW, 6-dB NF	[18], Nortel
Broadband amplifier	For optical networking receiver	Up to 50 GHz bandwidth in 7HP	[17], AMCC
High-gain amplifier	0.5-μm SiGe BiCMOS design	Integrated 60-dB stable gain for 12.5G	[19], Nortel
Dynamic frequency dividers	Building block, divide by 2	5HP – 50 GHz, 7HP – up to 98 GHz	Anonymous, unpublished
Multiplexer	For SONET applications	5HP – 12.5 Gb/s, 7HP – 56 Gb/s	[17, 20], IBM
Demultiplexer	For SONET applications	Up to 45 Gb/s	[17, 20], IBM
Ser/Des	0.5-μm single-chip solution	12.5 Gbaud	[21], IBM
Modulator driver	Distributed large-signal amplifier	Up to 48 Gb/s, 3.5 V peak-to-peak	AMCC data sheet
Network switch	68 × 69, 150000 SiGe HBTs	2.5 Gb/s, >200 Gb/s throughput	AMCC data sheet
10-Gb/s chip set	Complete chip set for STM64/OC-192 designed by Alcatel	Mux and demux, laser driver, preamp, limiting amp, CDR (data recovery)	[22], Alcatel
Data conversion			
D-to-A converter	Analog Devices design	12 bits, >1 GSample/s	[23], ADI
A-to-D converter	IBM Research	4 bits, 8 Gsample/s	[24], IBM
$\Delta\Sigma$ modulator	Fourth-order, 0.5-μm SiGe, LC resonators with Q enhancement	5 V, 350 mW at 4 GHz, max SNR 53 dB, SFDR 69 dB (11 bits)	[25], Carleton University

Continued on next page

Table 1 Continued.

Application/Circuit	*Comments*	*Figure of merit*	*Reference*
Memory			
Bipolar cache	RPI design	0.3 ns access time	[26], RPI
Ultrawide band			
Timing generator chip	0.5-μm SiGe HBT design	5 V, 0.5 W, up to 2.5 GHz, 2 ps accuracy, 10 ps jitter in a 100-ns window	[27], TDSI/SMI
Instrumentation			
Pin electronics driver			[28], IBM
Digital			
RISC engine	Simulation/analysis of methods to achieve >16-GHz RISC engine	SiGe higher HBT count and CMOS integration has major benefits	[29], RPI
Highly integrated			
OC48 mapper	0.5-μm SiGe BiCMOS	2.5 Gb/s highly integrated	[11], AMCC
ASIC test site	1.8M CMOS, ASIC qualification vehicle	Equivalent to base 0.5-μm CMOS	[30], IBM
Radar			
X-band phase shifters	PIN diode circuits with thick metal add-on module (Hughes/Raytheon)	2- and 3-bit fully integrated phase shifters at 6–10 GHz	[11], Hughes/IBM

resistors are being added [3]. The thrust for varactors is improved tunability, while maintaining linearity, and high Q (quality factor) values. Capacitors, both front-end-of-line (FEOL) MOS and metallization-based MIM, require higher capacitance per unit area to provide analog area scaling. The performance of spiral inductors continues to be improved by thick metals in spite of skin-effect concerns. Further enhancements include multiple layers of thick metal, deep-trench mazes under the inductor, and polysilicon ground shields.[4] These features, which are discussed in detail in the section devoted to passive elements, result in passives that are much better than those in conventional silicon CMOS and similar to passives in GaAs ICs.

Although the SiGe HBT transistor is the cornerstone of IBM BiCMOS technologies, many components contribute to their success. Moreover, there are applications which do not require the performance provided by the SiGe bipolar transistor. This application space was addressed by developing rf CMOS technologies as derivatives of the SiGe BiCMOS technologies. The first of these to be qualified, 0.25-μm CMOS 6SFRF, is based on the BiCMOS 6HP and CMOS 6SF technologies. RF CMOS technologies include an extensive suite of passive devices, device models optimized for radio frequency (rf) applications, and a design automation system which is compatible with rf design techniques. For CMOS devices, high-quality passives are critical in achieving a system on a chip (SoC), because of the difficulty of rf matching MOS devices. More advanced rf CMOS technologies are also being developed with minimum linewidths of 0.13 μm and 0.10 μm.

This paper first reviews the active devices (npn HBT and MOS FETs) and passive devices (resistors, capacitors, varactors, and inductors) available in these technologies in detail from a circuit designer's point of view. We present dc and ac figures of merit important for high-performance mixed-signal communications technologies. The tradeoffs involved in device design are also discussed. Included in this section is a discussion on the importance of electrostatic discharge (ESD) technology, with special requirements for rf applications. The next section covers technology development methodology for SiGe BiCMOS and rf CMOS devices. We discuss the qualification methodology and manufacturability of (Bi)CMOS mixed-signal rf technologies. This is followed by a discussion of other technology issues that have implications for circuit and product design. Noise, isolation, and active device reliability are discussed in detail, as well as metal electromigration, which is important for design of a reliable product.

2. Devices for communications technologies

SiGe HBT overview

The addition of Ge into the bipolar junction transistor (BJT) by IBM in the late 1980s, creating a heterojunction bipolar transistor, or HBT, enabled higher performance

[4] D. Coolbaugh, IBM internal communication.

than was believed possible in silicon technologies. A fundamental reason for using a BJT is its exponential change in output current with input voltage. At its peak operating point, the BJT achieves about three times the transconductance, and thus three times the drive capability, of an FET, as illustrated in **Figure 3**. Retaining the beneficial properties of the BJT, the incorporation of Ge into the base of the device introduced a number of further benefits.

Incorporation of substitutional Ge into the crystal lattice of the silicon creates a compressive strain in the material (because the Ge atom requires a larger atomic separation), and as a result, reduces the bandgap of the material. In a typical HBT (as in GaAs or InP materials), this bandgap difference between layers of semiconductor materials is used to affect the injection of carriers between the two sides of the junctions. Some SiGe HBTs are similar, where the Ge is formed in an abrupt transition to a constant value over a specified width. In the IBM "graded" SiGe HBTs, the Ge content is not a constant, but instead increases (low concentration closer to the wafer surface to high concentration deeper into the device) and thus contains a decreasing bandgap in the direction of electron flow. **Figure 4** is a schematic diagram of the Ge concentration and associated band structure illustrating this concept. The electrons are injected from the emitter of the device, having a reduced barrier to injection because of the small Ge content at the junction, and then experience an accelerating field from the increasing Ge content deeper into the device. The electrical effects of this graded Ge content are well documented [31]. The content at the junction increases the electron injection into the base, thus increasing the dc current gain. The Ge grade has the effect of speeding the transport of electrons across the device, resulting in higher-frequency operation. The Ge grade also improves the device Early voltage (flatness of the output current as a function of output voltage characteristics) by modulating the intrinsic carrier concentration across the base. The Gummel characteristic [**Figure 5(a)**] illustrates the fact that the turn-on voltage for a SiGe HBT compares favorably with III–V HBT devices, and the output characteristic [**Figure 5(b)**] illustrates very flat characteristics and a sharp "knee," both favorable to high voltage gain in such a device. The aspect of acceleration of electrons across the device is one of particular importance in scaling the device to higher-speed performance, as is discussed shortly.

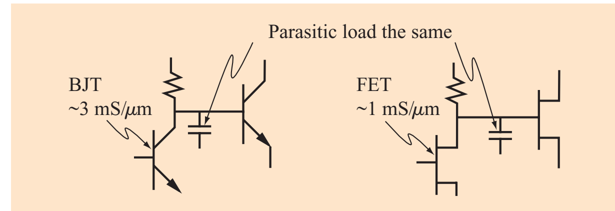

Figure 3

Bipolar junction transistor (left), with three times higher transconductance, more effectively drives a parasitic load than a field-effect transistor (right).

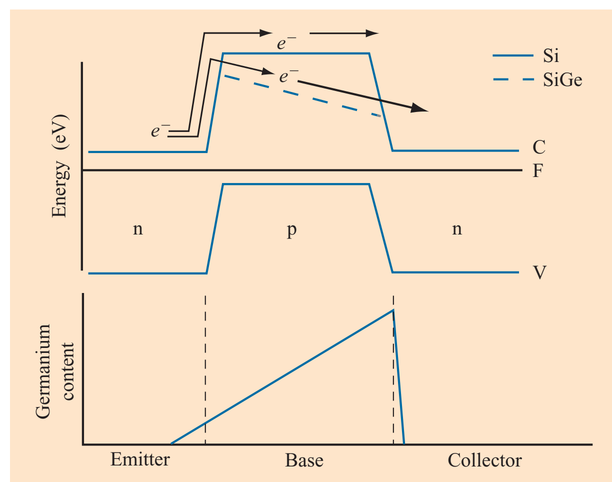

Figure 4

Ge concentration (bottom) and band structure (top) of a SiGe heterojunction transistor. The Ge provides a lower barrier to injection from emitter to base as well as an accelerating field through the base.

HBT device design

Today, IBM is engaged in a number of SiGe HBT device design activities, driven by markets with differing requirements (see the summary of HBT characteristics in **Table 2**). Even though high-speed performance often gets the attention in SiGe HBT device developments, advances are taking place to address applications that do not demand higher speed but rather higher-voltage operation or lower costs.

Semiconductor chips used in wireless applications such as cellular phones, wireless networks, and global positioning systems (GPSs) are required to be inexpensive. The number of masks and the complexity of processing affect wafer cost and yield, and therefore the final packaged part cost. To achieve cost reductions, wafer processing is simplified by reducing the number of process steps. These reductions can take the form of eliminating a portion of the structure (deep-trench isolation), consolidation of masking steps, or changes to the HBT structure [non-self-aligned (NSA) extrinsic base]. In all

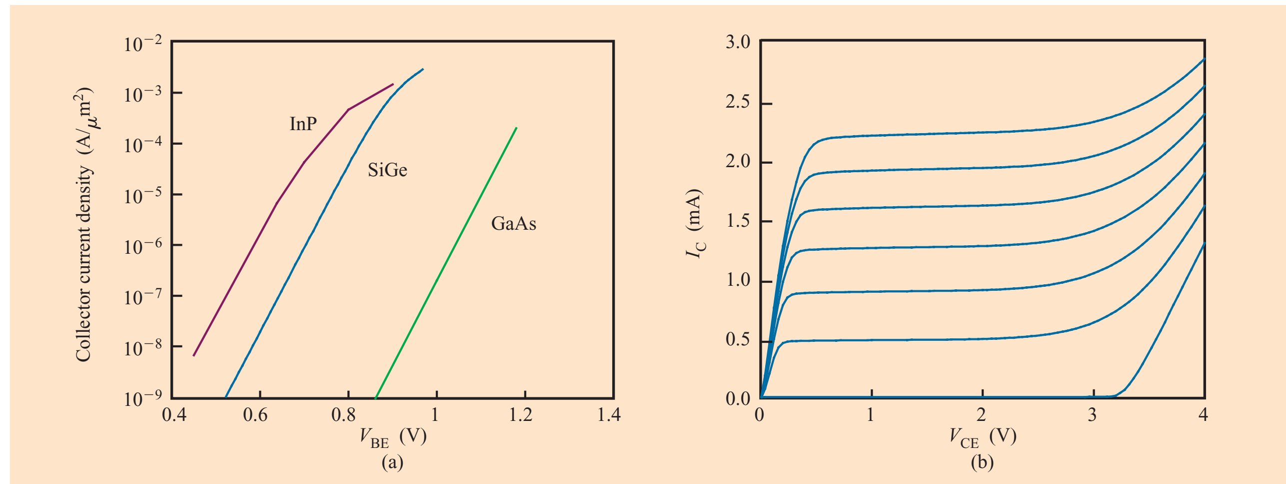

Figure 5

(a) Gummel characteristic of SiGe HBT demonstrates linear characteristics and low turn-on voltage. (b) Output characteristic demonstrates flat I_C versus V_{CE}, enhancing voltage gain in applications.

Table 2 HBT characteristics across generations of BiCMOS technology.

	Units	*5HP*	*5HPE*	*6HP*	*7HP*	*8HP*
npn isolation		Deep trench	Shallow trench	Deep trench	Deep trench	Deep trench
Peak f_T	GHz	50	45	50	120	210
Peak f_{max}		65	50	65	100	185
f_T at 30 μA (min. area)	GHz	15	19	19	25	50
I_C at peak f_T (min. area)	mA	0.6	0.5	0.5	1.0	1.0
BV_{CEO}	V	3.3	3.3	3.3	2.0	1.9
BV_{CBO}	V	10.5	10.5	10.5	6.5	6
Peak f_T High-*BV* npn	GHz	29	17	29	20	—
BV_{CEO} High-*BV* npn	V	5.5	10.0	5.0	4.7	—
BV_{CBO} High-BV npn	V	14.0	20.5	14.0	12.5	—
npn density (min. area)	relative units	1×	1×	1.7×	2.0×	2.0×

situations, the device performance is altered as part of the device customization required for a particular end use.

An example of the cost/performance tradeoff is illustrated by the SiGe 5MR technology, which was tailored for the ±5-V supply voltage used by hard disk drive preamplifiers. These enhancements were also incorporated into SiGe 5HPE. Again, the chip cost was required to be low, and the challenge was to meet both the cost and use voltage criteria simultaneously. While the higher BV_{CEO} target (9.6 V) was met by increasing the lightly doped collector epitaxial layer thickness, the output characteristics of the high-breakdown HBT suffered from barrier effects [32] caused by base broadening, as shown in **Figure 6(a)**. The usual high values of Early voltage were

compromised. Two approaches were taken to improve transistor performance: 1) improve the base Ge profile by introducing the boron within the Ge base layer, and 2) increase the lateral spacing between the extrinsic base implant with respect to the emitter opening, thus decreasing enhanced diffusion of the intrinsic base caused by the extrinsic base implant [33]. These two improvements resulted in a substantially improved V_A, as shown in **Figure 6(b)**. In addition, the peak frequency performance, f_T, was improved from 14 GHz to 19 GHz.

With an increased distance from the extrinsic base implant to the emitter opening, it was more cost-effective to simplify the usual self-aligned extrinsic base structure to a NSA version in which the emitter polysilicon itself was used as the mask for the extrinsic base implant. A 7% reduction in processing time and an equally substantial reduction in wafer cost were achieved. These device improvements were feasible because the circuit designers were willing to trade off higher base resistance for increased frequency performance and Early voltage. Owing to the less complex emitter definition process, the V_{BE} matching is also markedly improved. These device tradeoffs meet both the circuit design and wafer cost requirements and demonstrate the versatility of the successful IBM SiGe technologies.

In the high-speed arena, SiGe HBTs today are surpassing even the fastest III–V production devices. The key to this achievement is the superior within-device parasitic-control technology available to SiGe device designers, compared to what is available to III–V device designers. With lithographically defined implants, trench isolation, self-aligned low-resistance regions, and options such as spacer technology, silicon device designers have a myriad of tools at their disposal.

The most common measure of performance is f_T, which is the maximum frequency at which the transistor demonstrates useful (i.e., above unity) *current* gain. The components of f_T are the diffusion capacitance charging relation $(kT/qI_E)(C_{EB} + C_{CB})$, transit times across the device (principally consisting of base transit time τ_B and collector space-charge transit time τ_C), and the collector resistance–collector base capacitance $R_C C_{CB}$ charging time, as shown in Equation (1):

$$1/(2\pi f_T) = \tau_{EC} \cong (kT/qI_E)(C_{EB} + C_{CB}) + R_C C_{CB} + \tau_B + \tau_C. \quad (1)$$

Improvements in f_T are achieved by reducing the thickness of each of the layers through which the electrons must travel—the neutral base (i.e., affecting τ_B) and the collector space-charge region (i.e., affecting τ_C), as well as reducing the RC charging terms for the parasitic capacitances in the device. This concept is shown in **Figure 7(a)**. The distribution of the boron dopant (which comprises the base) is made narrower; the Ge distribution is also made narrower, and the grade is increased; also, the

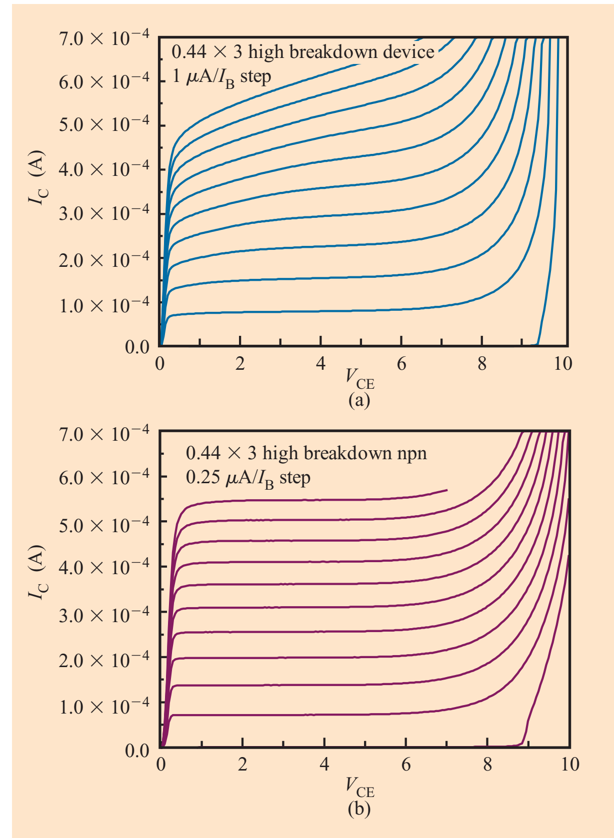

Figure 6

Output characteristics (a) prior to and (b) following Ge profile and extrinsic base modifications in the 5HPE technology.

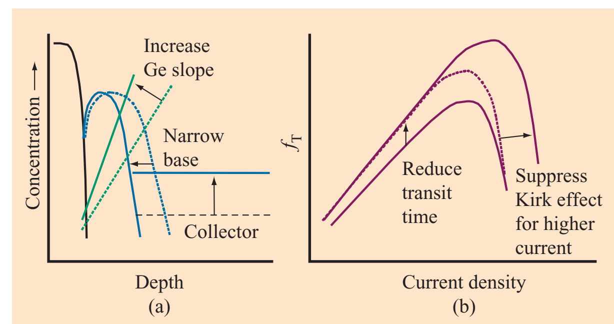

Figure 7

Vertical scaling of the graded-base SiGe HBT: (a) Dopant profile is made more narrow for reduced transit time and reduced collector resistance. (b) Relationship between f_T and current density.

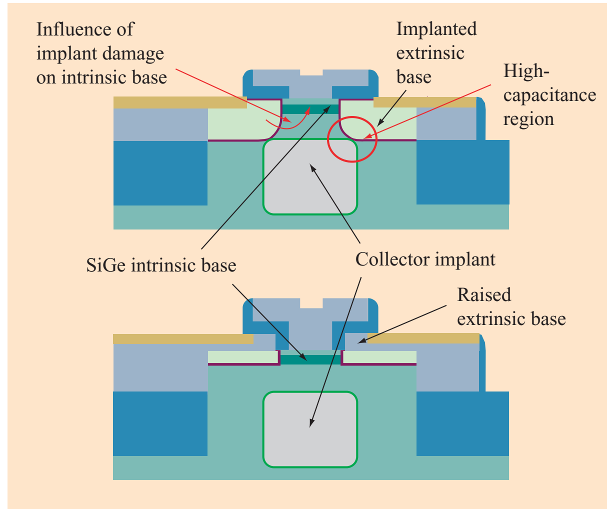

Figure 8

ETX structure (top) and RXB structure (bottom). The RXB structure eliminates the unwanted effects from the deep implant, including the excess capacitance and diffusion effects on the intrinsic base region.

collector concentration is increased, which reduces the thickness of the space-charge region and at the same time reduces the collector access resistance. We refer to this as vertical scaling of the transistor, since these aspects are not related to the lateral dimensions of the device. The result of vertical scaling is to reduce the transit time and increase the maximum operating current density in the device (i.e., for the same size device, the current to reach maximum f_T performance is increased). **Figure 7(b)** shows this effect of vertical scaling on a plot of f_T vs. current density.

The second common measure of performance is f_{max}, which is the maximum frequency at which the transistor has useful (i.e., above unity) *power* gain; f_{max} is approximately given by the well-known relationship between f_T and parasitics,

$$f_{max} \cong (f_T/8\pi R_{BB}C_{CB})^{1/2}, \quad (2)$$

where R_{BB} and C_{CB} are respectively the parasitic base resistance and collector–base capacitance. For most applications, it is required that the f_{max} value be at least comparable to the f_T value for optimal circuit performance. Achieving high f_{max} is a challenge from the point of view of both device design and process, since it is a strong function of the device structure, which largely determines the values of R_{BB} and C_{CB}. This is because the majority of R_{BB} and C_{CB} are present in the extrinsic part of the device, or that region of the device which is not an essential part of the carrier transport. This fact provides the expectation that f_{max} will continue to be substantially improved with new device structures.

Comparison of the IBM SiGe HBT device structures illustrates how improvements in device structure may provide increases in the figure of merit, f_{max}. Through several generations of technology, IBM has utilized the same device structure, often referred to as the epitaxial transistor (ETX). Its identifiable structural characteristic is an extrinsic base implanted into the SiGe epitaxial film. Through careful analysis, depending heavily on 2D simulations [34], it was determined that this structure has some significant limitations. Implants into the silicon create lattice defects, which affect the diffusion of the intrinsic base boron, increasing τ_B and thus reducing device performance. This limits how close the implant may be placed to the intrinsic device, and therefore creates a lower limit on the achievable base resistance, R_{BB}. The implanted extrinsic base also extends deep into the silicon and intersects the collector implants at a high concentration, which results in high C_{CB}. Shown in **Figure 8** are the ETX structure and the structure IBM is pursuing with a raised extrinsic base (RXB) to substantially reduce R_{BB} and C_{CB}. The raised extrinsic base has less influence on the intrinsic dopant diffusion and may be placed in close proximity to the intrinsic device, thus reducing R_{BB} without impact to f_T. It also has a minimal junction depth, and, as such, has a relatively small C_{CB}.

Initial results on the RXB structure demonstrate its benefits over the ETX structure. While retaining the f_T performance of a structure without a self-aligned extrinsic base (indicating no influence of the extrinsic base on the intrinsic base), the base resistance has been reduced by a factor of approximately 2, and C_{CB} has been maintained constant compared to a previous-generation device of similar area, with lower f_T. This results in simultaneous f_T and f_{max} improvements between generations of more than 80% (**Figure 9**).

FETs and their utility

The CMOS device takes on different roles whether offered as part of a BiCMOS technology, where the bipolar device is available for analog functions, or as part of a CMOS-only technology, where the FET devices must take a primary role in analog functionality. From device design, device layout, process development, characterization, and modeling, this differentiation influences technology development. This section discusses not only the digital design aspects of FET devices, but also aspects that are driven by analog requirements, such as the ability of these devices to withstand higher voltages or have lower back-bias sensitivity (body effect) or higher self-gain (g_m/g_0). These aspects were less important in BiCMOS processes because of the presence of the bipolar

device, but in CMOS-only technologies they become more essential. Thus, one finds as a requirement that additional masks and complexity be present in CMOS processes, and a greater variety of FET devices are offered to designers.

When offered as part of IBM SiGe BiCMOS technologies, the CMOS devices are used primarily for integrating digital logic functions with high-speed bipolar analog circuits. This allows fully integrated system-on-a-chip products, with the CMOS performing the lower-frequency baseband signal processing. The logic functionality is streamlined by offering ASIC library elements from the base CMOS technology to be integrated with the rf analog circuits. The CMOS devices can also be used for low-frequency analog functions such as A-D converters, multiplexers, and switches. CMOS devices have one large advantage over bipolar devices: There is essentially no gate current. This makes CMOS devices ideal in circuits where it is required to measure the charge on capacitors such as A-D converters. Bipolar devices would drain the charge during the measurement.

Development of CMOS devices for digital logic purposes is driven primarily by shrinking the device dimensions, thinning the gate oxide, and lowering supply voltages to achieve faster performance, increased density, and lower power consumption. The smaller device lengths lower the parasitics and increase f_T, but also necessitate complex designs including halo implants to minimize short-channel effects and control punch-through. These implants have negative effects on important analog characteristics such as self-gain (g_m/g_0). Also, the thinner gate oxides in the advanced logic devices cannot support the higher voltages required in analog circuits. Additionally, gate current becomes non-negligible. The solution to this is a dual-oxide technology. The analog devices are designed with thicker oxides, longer channel lengths, and unique source/drain extensions. This added process complexity allows placement of high-performance logic devices and high-voltage analog devices on the same chip.

Some specific parameters such as noise and V_t matching must be considered when designing analog CMOS devices. Noise is not a large concern in digital CMOS circuits, and some processes such as nitrided gate oxide actually increase noise in a tradeoff for decreased dopant penetration of the gate oxide and improved hot-carrier degradation. V_t matching in analog circuits is much more critical than in logic circuits, and all variables that introduce mismatch, including process and layout, must be minimized.

IBM has four SiGe BiCMOS technologies and one CMOS rf technology qualified for high-volume production:

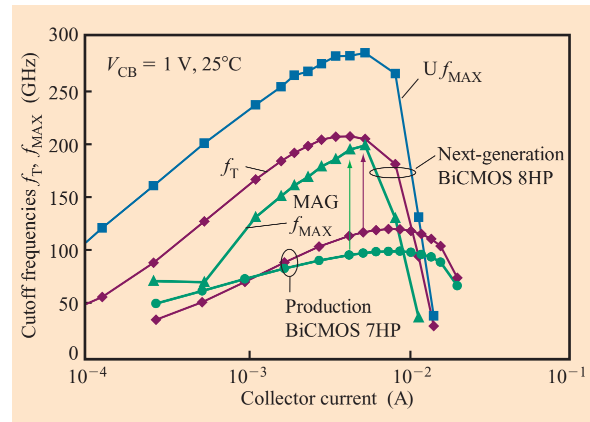

Figure 9

Comparison of cutoff frequencies between SiGe 7HP f_T = 120-GHz device with ETX structure and next-generation f_T = 210-GHz device, with vertically scaled profile and new RXB structure. (MAG = maximum available gain; U = unilateral matched power gain.)

SiGe 5HP, SiGe 5HPE, SiGe 6HP, SiGe 7HP, and CMOS 6SFRF. SiGe 5HP and SiGe 5HPE are single-gate-oxide technologies, while the rest have an optional dual-gate-oxide process. SiGe 5HP contains 3.3-V CMOS devices designed specifically for logic support in the BiCMOS technology. SiGe 5HPE has a 12-nm gate oxide, 5-V CMOS with an additional isolated n-FET device. The iso-n-FET is a standard n-FET surrounded by an isolation tub which allows the iso-n-FET p-well to be biased independently from the substrate. Independent well biasing enables a circuit designer to handle dual logic levels on-chip, for example by biasing the substrate at −5 V and the p-well in the tub at 0 V. Higher-voltage analog signals can also be handled in this way by stacking 5-V FETs inside and outside the isolation, with a 10-V signal across the combination. Iso-n-FET devices also have better noise isolation owing to the independently biased p-well and isolation tub.

The dual-oxide technologies are SiGe 6HP, CMOS 6SFRF, and SiGe 7HP. SiGe 6HP contains 2.5-V and 3.3-V CMOS devices, which have 5-nm and 7-nm gate oxides, respectively. The thin-oxide FETs, with 0.25-μm L_{min} (minimum drawn gate lengths), are used for the high-speed logic, while the thick-oxide devices are 0.4-μm-L_{min} n-FETs and 0.34-μm-L_{min} p-FETs. The thick-oxide FETs enable 3.3-V I/O compatibility as well as analog signal handling. CMOS 6SFRF is based on the same 2.5-V/3.3-V devices, with an additional 2.5-V iso-n-FET and a process option of 6.5-V thick-oxide (14-nm) devices in place of the 3.3-V devices. The 6.5-V devices have L_{min} = 0.7 μm to support the higher voltage. These devices can be used

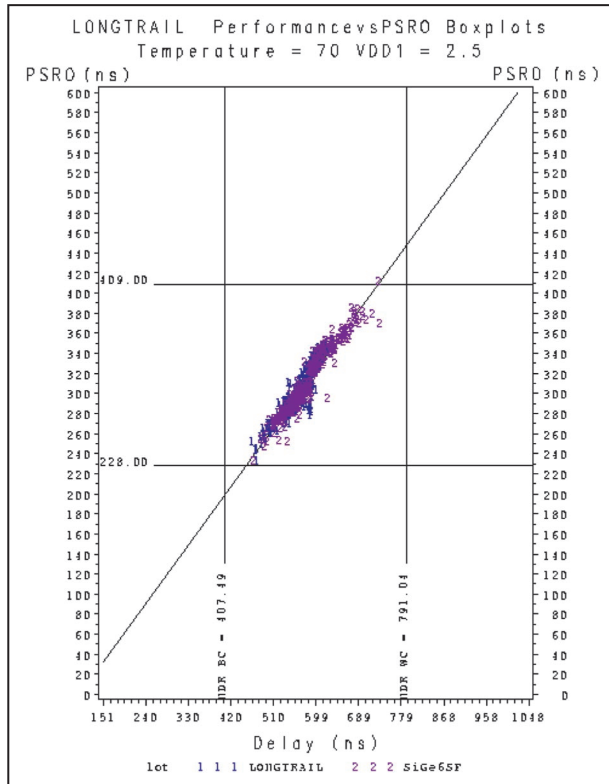

Figure 10

Box plot showing SiGe 6SF CMOS performance sort ring oscillator (PSRO) (2) identical to CMOS 6SF Longtrail hardware (1).

as low-frequency power amplifiers (amps), high-voltage analog switches, and voltage regulators in battery chargers. SiGe 7HP has 1.8-V and 3.3-V CMOS devices with 3.5-nm and 6.8-nm gate oxides, respectively. There are 1.8-V standard-V_t FETs and optional 1.8-V high-V_t FETs, 3.3-V FETs, and both 1.8-V and 3.3-V iso-n-FETs. The 1.8-V FETs have $L_{min} = 0.18$ μm and the 3.3-V FETs have $L_{min} = 0.4$ μm. **Table 3** compares some of the key parameters of each technology.

The main purpose of the CMOS devices in a BiCMOS technology is to provide integrated logic functionality. The logic design can be expedited by using ASIC library "books" already developed for the base CMOS technology. This approach can be used only if the CMOS device characteristics in the BiCMOS technology closely match those of the base CMOS technology. Many process differences can lead to significant device differences. Adjusting the process minimizes many of these differences, but some cannot be corrected. To verify that the ASIC library elements function correctly and that the CMOS timing models are still valid for the BiCMOS process, ASIC library test sites are built in the BiCMOS process. The chips are tested for functionality, and hardware-to-model correlation is done to validate the timing models. Because some devices are known not to function correctly owing to process differences, any library elements containing these devices are not tested. In **Figure 10**, a typical correlation plot with both SiGe and CMOS data shows that the same model can accurately represent both technologies.

Table 3 Comparison of thin-oxide CMOS parameters for SiGe BiCMOS and rf CMOS technologies.

Parameter	*Units*	*SiGe 5HP*		*SiGe 5HPE*		*SiGe 6HP*		*SiGe 7HP*		*CMOS 6SFRF*	
		n-FET	*p-FET*	*n-FET*	*p-FET*	*n-FET*	*p-FET*	*n-FET*	*p-FET*	*n-FET*	*p-FET*
T_{OX} (thin)	nm	7.8		12.0		5.0		3.5		5.0	
T_{OX} (thick)	nm	—		—		7.0		6.8		7.0/14.0	
V_{SUPPLY}	V	3.3		5		2.5/3.3		1.8/3.3		2.5/3.3/6.5	
L_{min}	μm	0.5		0.5		0.25		0.18		0.25	
L_{EFF}	μm	0.39	0.36	0.4	0.45	0.19	0.18	0.12	0.14	0.18	0.18
$V_{T lin}$	mV	600	−550	820	−740	500	−500	355	−420	500	−500
$I_{D sat}$	μA/μm	480	213	600	265	595	280	600	260	595	280
I_{OFF}	nA/μm	0.1	0.1	0.004	0.003	0.005	0.003	0.1	0.05	0.005	0.003
Body effect		0.34	0.35	0.15	0.23	0.23	0.27	0.19	0.25	0.23	0.27
$g_{m sat}$	μS/μm	195	103	165	78	300	200	500	275	300	200
f_T	GHz	20	10	19	9	35	20	75	45	35	20
f_{max}	GHz	22	17	—	—	22	22	70	45	22	22

Table 4 Electrical parameters of resistors available in SiGe and rf CMOS technologies.

Resistor	*Sheet resistance* (Ω/□)	*Tolerance* (%)	*TCR* (ppm/°C)	*Parasitic capacitance* (fF/μm^2)	*Maximum current* (mA/μm)
p+ polysilicon	270	10–15	21	0.11	0.6
p polysilicon	1600	25	−1105	0.09	0.1
n+ diffusion	72	10	1751	1.00	1.0
n subcollector	8	15	1460	0.12	1.0
TaN metal	142	10	−728	0.03	0.5

High-quality passive components critical for communications circuits

BiCMOS technology development in IBM has been focused largely on the integration of high-performance SiGe HBTs in a base CMOS technology. In general, passive devices are developed from existing processes used for these transistors; i.e., resistors are formed from CMOS FET source/drain implants, MOS capacitors from the reach-through implants used for the HBT collector contact and FET gate oxide/polysilicon gate, and inductors designed using last-metal options for these technologies. The need for high integration and technology innovation in rf circuit design has changed the direction of passive development in the last several years. Passive devices which in some cases utilize processes not used for transistor manufacture have allowed the development of high-performance devices enabling rf technology innovations. Examples are thick analog metals (AMs), e.g., 4-μm Al, used as last-metal options for high-Q inductors; TaN resistors integrated in the back-end-of-line (BEOL) metallization for low parasitic capacitance/tolerance; and high-capacitance nitride metal-insulator-metal (MIM) capacitors.

Balancing the performance of passive devices with processing costs is a challenge. Some of the more critical parameters for the passive elements used in rf designs are resistor tolerance, varactor tunability (C_{max}/C_{min}) and linearity, MIM capacitance density and quality factor (Q), and inductor Q. In the following sections, the important passive elements offered in the IBM SiGe BiCMOS and rf CMOS technologies are described, with focus on their rf application, key figures of merit, and reliability.

Resistors

Resistors are used in all analog and mixed-signal circuit blocks. A wide variety of resistors are offered in the IBM SiGe BiCMOS and rf CMOS technologies to accommodate designer needs (see **Table 4**). Figures of merit for resistors are sheet resistance, tolerance, parasitic capacitance, voltage, and temperature coefficients. Three types of basic resistors are used in the SiGe BiCMOS process to achieve the desired properties and resistance ranges needed in analog circuit designs: p-doped polysilicon resistors, n- and p-type diffusion resistors, and BEOL TaN metal resistors.

Highly doped p-type polysilicon resistors are preferred in most cases for mixed-signal and analog applications because of their good matching, low parasitic capacitance to the substrate, and excellent temperature coefficient, as shown in Table 4. These resistors consist of gate or SiGe polysilicon doped with a high-dose boron implant, normally the p-FET source/drain implant. Either shallow-trench isolation or shallow/deep-trench isolation is used under these resistors to reduce parasitic capacitance between the resistor and substrate. The ends of the resistor are silicided for low contact resistance to the BEOL wiring, and the body of the resistor is covered with silicon nitride to block the silicide. The p+ polysilicon resistor has a sheet resistance of 270 Ω/□ and a 10–15% tolerance. Low tolerance is essential for efficient compact circuit designs. Table 4 shows that this resistor has a very low temperature coefficient (TCR) of 21 ppm/°C, which is 2–3% the TCR of the other resistors offered. This makes the resistor most attractive for circuit applications owing to low variation in resistance with changes in temperature over typical ranges of −40°C to 125°C. The parasitic capacitance between the resistor and substrate is 10% of that of a diffusion resistor but four times the value for a BEOL resistor because of the distance of these devices from the substrate. A low-doped p-type polysilicon resistor is offered in these technologies as well. This provides a higher sheet resistance at 1600 Ω/□ for applications requiring high resistance while maintaining good parasitic capacitance. This resistor is more difficult to control in the process, resulting in a 25% tolerance.

The n+ diffusion resistor is formed with the n-FET source/drain implant in single-crystal silicon. The ends of the resistor are silicided. With a sheet resistance of 72 Ω/□, the n+ diffusion resistor is used in current source/biasing circuits where resistors in the range of 50–100 Ω are needed. Since this resistor is made from the FET source/drain, it has a high capacitance which limits its use. This resistor is typically controlled to a 10% tolerance.

An NS resistor is made from the low-resistance npn subcollector and contacted with the collector contact. This

device has a low sheet resistance at 8 Ω/□ and a tolerance of 10–15%. Typical of diffusion resistors, this device has a high temperature coefficient at 1460 ppm/°C. This resistor is ideally used as a ballast resistor in applications such as power amplifiers.

A thin-film BEOL resistor has several attractive features, such as low tolerance, low parasitics, and the ability to make design changes with short lead times. A TaN resistor is offered in several of the IBM SiGe BiCMOS technologies at metal levels M1 and M5. This device consists of a TaN film contacted by metal vias. The tolerance is low at 10%, and because of its distance from the substrate, it has very low parasitic capacitance to the substrate.

All resistors offered in the IBM SiGe BiCMOS and rf CMOS technologies meet stringent reliability requirements for 100000 power-on hours. Reliability tests are performed by measuring the shift in resistance over a fixed period of time under constant current. By varying the bias conditions used to stress these devices, the amount the resistor will shift in 100000 hours can be projected. Typically, resistance changes of less than several tenths of a percent are projected over the life of the resistor for the current limits specified in Table 4. Current limits of 1 mA/μm of width for diffusion resistors are normal. Low-resistance polysilicon and BEOL resistors have a current limit of 0.5–0.6 mA/μm.

Capacitors

Passive devices, such as inductors, resistors, and capacitors, dominate the component count in modern wireless appliances. A passives-to-active device ratio of 20:1 is commonplace on a typical off-the-shelf cellular phone [35]. To reduce form factors of handheld devices, traditional surface-mounted passives are being integrated into the chip. Three types of capacitors have been developed in SiGe technologies to meet customer requirements for reduced board-level components. MOS (polysilicon gated capacitors on single-crystal silicon), PIP (polysilicon-insulator-polysilicon), and MIM (metal-insulator-metal) capacitors each have their own place for use in different application spaces depending on capacitance desired and performance at the application frequency. An overview of process details for optimization, electrical performance, and reliability will be given for each device.

The simplest MOS capacitors are formed without additional masks from the FET elements in all SiGe BiCMOS generations using silicided gate polysilicon, thin gate oxide, and FET well-doped silicon. Although these devices have a very high capacitance per unit area owing to the ultrathin oxide, they are not particularly useful for rf applications because of the high resistance of the well doping (~250 Ω/□) and poor voltage coefficient. A more optimized capacitor has been developed by heavily doping the silicon substrate to reduce parasitic resistance [2]. This is accomplished by using a high-dose phosphorus reachthrough implant (~25 Ω/□) to dope the bottom plate of the capacitor. During gate oxidation, the insulator grown over high-dose phosphorus implants can result in a 50–100% increase in thickness relative to oxides grown over intrinsic silicon because of enhanced oxidation. Shallow reachthrough implants can cause unreliable oxides due to very high growth rates driven by high surface-dopant concentrations. The quality of oxide grown over the diffusion region increases significantly with implant depth. A comparison of the applied field in depletion mode at a 1-nA leakage current showed that a shallow implant causes premature oxide leakage (at 5.2 MV/cm) relative to the deeper implant (6 to 7 MV/cm), which meets leakage requirements. Therefore, an optimized MOS capacitor will have a high-dose reachthrough implant at a moderate depth for low resistance and a reliable oxide.

PIP capacitors are fabricated in double-polysilicon BiCMOS processes [36]. The unit capacitance is a product of the integration methodology, and typically the device does not require an additional process step. Fabricated only in SiGe 5HPE, the capacitor structure is formed using p+-doped gate polysilicon as the bottom plate, a deposited oxide layer for the capacitor dielectric, and silicided extrinsic base polysilicon as the top electrode. To minimize the bottom-plate capacitance to substrate, the doped gate polysilicon is patterned over shallow-trench isolation and/or deep-trench maze, an advantage gained over the MOS structure. The dielectric quality is critical to ensure high reliability and robust breakdown strength. Thermal oxides are rarely used, because the polysilicon roughens along grain boundaries during oxidation, yielding high field points that reduce the breakdown strength. An obvious alternative is PECVD dielectric, but these dielectrics typically have poor uniformity, poor conformality, and pinholes in thin films. For this application, a thin deposited hot thermal oxide (HTO) was developed. The HTO breaks down in the range of 9–10 MV/cm and is very conformal, yielding full thickness coverage at the gate polysilicon corners where premature breakdown can occur under high electric fields. Optimizing linearity for the PIP capacitor was an important aspect of its development. To understand C–V linearity as a function of dopant type and dose, experiments were designed which varied dopant type and concentration for each of the capacitor electrodes. The total capacitance and linearity are a function of the polysilicon depletion capacitance in series with the dielectric capacitance. In the optimal electrode configuration, both plates of the device are doped n-type. At a given bias, one plate is in depletion while the other plate is in accumulation, causing

a small change in the net capacitance. In contrast, when one plate is doped n-type and the other p-type, the plates are simultaneously in either depletion or accumulation, causing a larger change in the net capacitance, which results in reduced linearity.

While acceptable for use in low-frequency applications, MOS and PIP capacitors suffer from low quality factors (Qs) due to high-resistance plates and capacitive losses in the 2–10-GHz range, rendering them nonideal or limiting their use. A novel metal-insulator-metal capacitor (MIMCAP) was developed which takes advantage of low-resistivity metal wiring and of a thick interlevel dielectric which physically distances the devices from the relatively low-resistivity substrate and the planar back-end-of-line (BEOL) topology in order to build in high reliability [37]. The SiGe BiCMOS planar MIM (**Figure 11**) is fabricated by depositing a 50-nm PECVD oxide and a 200-nm metal stack on top of any metal wiring level except the first and last. A mask is applied and the top plate is etched, stopping at the capacitor dielectric. The metal layer mask, which defines the metal wiring as well as the base capacitor plate, is then applied. An interlevel dielectric is deposited and planarized, and vias added to connect to the next metal layer. The dielectric of the MIM capacitor is thicker than those of either PIP or MOS capacitors because lower-temperature dielectrics (compatible with BEOL processing) are generally of poorer quality than higher-temperature CVD or thermal oxides.

Designers prefer the MIM capacitor over the other two types because of its advantageous performance (higher Q) at higher frequencies. Thick metal plates offer lower resistance than doped and/or silicided polysilicon, and placement in the interconnect levels significantly reduces the parasitic capacitance of the substrate. Finally, the ability to resize the MIM in a BEOL redesign reduces cycles of learning, a benefit not available with silicon-based capacitors. The penalty paid for these benefits is that a large area of the chip is consumed, affecting the ability to reduce the form factor of the chip. Capacitors may require as much as 50% of the chip area, depending on the application. In order to decrease the capacitor footprint, several options to increase the unit capacitance are available, since capacitance is a direct function of the dielectric constant of the insulator and is inversely proportional to film thickness.

The list of requirements which a high-dielectric-constant material must meet in order to address manufacturing, yield, design, and reliability concerns is a long and demanding one. **Table 5** contains a short list of critical parameters. From a fabrication aspect, the deposition process must meet manufacturability targets, have slow and controllable deposition rates, have high throughput, and have no impact on BEOL yield or parametrics. From a design aspect, the new dielectric should not significantly change ac device models established from prior generations. Finally, the film must have low defect density and negligible fixed or mobile charges, and it must be stable under thermal stress in order to pass stringent reliability qualification.

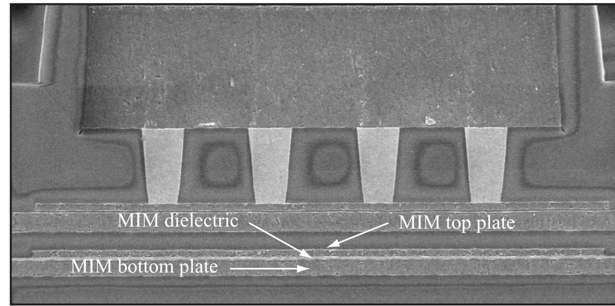

Figure 11

Cross-sectional SEM micrograph of MIM capacitor in SiGe BiCMOS technology.

Table 5 Critical parameters for high-k dielectrics required for MIM capacitors.

Property	*Value*
Deposition temperature	<400°C
Thickness uniformity	<5% (3σ)
Deposition rate	30–50 nm/min
T_{CC}	<30 ppm
V_{CC}	<100 ppm
Operating voltage	±5 V
Reliability	<10 ppm at 100K POH
Leakage	10^{-6} A/cm^2 at ±5 V
Dielectric constant	7 to 25

T_{CC} = temperature coefficient of capacitance; V_{CC} = voltage coefficient of capacitance.

A processing limitation for all new dielectrics will be deposition temperatures of ~400°C or less to prevent the shorting of narrowly spaced large metal lines due to metal extrusions. PECVD nitrides are known for their relatively high hydrogen content, bonded to both silicon and nitrogen. Recently, a PECVD nitride has been qualified which increases the capacitance per unit area by 43% over prior oxide dielectric. Aluminum and tantalum oxide processes are coming on line, driven primarily by next-generation CMOS gate-oxide replacement and DRAM node capacitors. These deposition processes cover the spectrum from atomic layer to bulk CVD, and often require clustering with rapid thermal process modules to fully oxidize the unreacted carbon compounds derived from the source material. Very-high-k and ferroelectric films such as composites of barium, strontium, bismuth, and titanium are still two to three generations away from implementation [38].

Table 6 Summary of key parameters for capacitors offered in SiGe technologies.

Capacitor	*Parameter*	*SiGe 5HP/AM/DM*	*SiGe 5HPE*	*BiCMOS 6HP*	*BiCMOS 7HP*
MOSCAP	Capacitance at 0 V (fF/μm^2)	1.5	1.2	3.1	2.5
	Tolerance (%)	10	15	15	15
	T_{CC} (ppm/°C)	48	21	20	—
	V_{CC} (+5/−5V ppm/V)	1740/1740	−990/−450	−7500/−1500	−5480/−1240
Poly-Poly	Capacitance at 0 V (fF/μm^2)	—	1.6	—	—
	Tolerance (%)	—	25	—	—
	T_{CC} (ppm/°C)	—	21	—	—
	V_{CC} (+5/−5V ppm/V)	—	−3525/−2475	—	—
MIM	Capacitance at 0 V (fF/μm^2)	0.7	1.35/2.7	0.7/1.4	1.0
	Stacking	Single	Double	Double	Single
	Tolerance (%)	15	15	15	15
	T_{CC} (ppm/°C)	−57	−44	−44	−15
	V_{CC} (+5/−5V ppm/V)	$<$25	$<$25	$<$25	$<$25

Finally, by taking advantage of the planarity and modularity of integration, wiring MIM capacitors in parallel on two or more levels can yield an equivalent multiple increase in unit capacitance, albeit at the cost of a mask level for each. Similarly, in SiGe 5HPE, the MOSCAP and PIP capacitors can be integrated into one structure and wired in parallel to yield a total unit capacitance of 2.8 fF/μm^2.

The planar MIMCAP concept and fabrication techniques have been successfully transferred to all SiGe generations as well as CMOS 5/6 technologies. The fabrication strategy has also been used to integrate the device into copper BEOL (CMOS 7/8) [39]. The integration of more advanced CMOS technologies into a copper BEOL presented many challenges that ultimately resulted in a process similar to that of the aluminum MIMCAP. Approaches using the copper level as the bottom plate in a fashion analogous to the aluminum approach were not successful because of issues associated with copper metallurgy (formation of hillocks or extrusions), the requirement of large copper areas for oxide plugs for chemical-mechanical polishing (CMP) in order to achieve planarity, and because copper was oxidized during the deposition of a dielectric which required oxygen, thereby precluding the direct deposition of all oxides. The so-called MOD (MIM over dielectric) provides a planar starting surface, relief from copper exposure to oxidizing and chlorine etch ambient, and capacitor size constraints. Plate materials and thickness are designed to be able to fit within the dual damascene stack while not affecting wiring and via parametrics and yield.

Table 6 summarizes key parameters for the optimized capacitor structures, comparing capacitance per unit area temperature linearity (T_{CC}) and voltage linearity (V_{CC}). The polysilicon-insulator-polysilicon (poly-poly, or PIP) capacitor has improved parasitics relative to the MOS capacitor because it is over shallow-trench isolation (STI). Area capacitances of the bottom plate to substrate are 1/10 the parasitics for the bottom plate of the MOS capacitor. The PIP capacitor can have a reduction in bottom-plate-to-substrate parasitics for a device over STI/deep trench (DT) relative to a device over STI only. Because the MIM capacitor is produced in the BEOL, it has the lowest parasitics of the devices described. The area capacitance of the bottom plate to substrate is significantly lower than that for the PIP capacitor over DT when the MIM is at M5. However, the MIM perimeter parasitics are much higher. In the 2–4-GHz frequency range, the MIM has the highest Q of the devices described. For a 20-μm $\times$ 20-μm device, the MIM has a Q of 90 and the MOS capacitor a Q of 20. A comparison of the MOS and PIP capacitors for a 10-μm $\times$ 50-μm device shows Q values of 3 and 6, respectively.

Reliability is central in the design and development of capacitors for BiCMOS technologies. The goal is to maximize capacitance by reducing dielectric thickness while still maintaining acceptable reliability at the rated use voltage. Capacitor reliability is determined using a time-dependent dielectric breakdown (TDDB) test. The devices are biased at high electric fields to accelerate the time to failure. The failures are plotted as a Weibull distribution plot at multiple stress voltages, and then

converted to a lifetime plot (**Figure 12**) to extrapolate to 100000 power-on hours to determine the electric field the capacitor will survive for this period of time. The MIM capacitor is less reliable than the MOS or PIP capacitors. This result is expected, since the MIM oxide is a PECVD oxide, while the MOS and PIP capacitors are higher-quality oxides. Therefore, the MIM must have a thicker oxide and lower capacitance to meet the same reliability requirements. Also, the PIP capacitor shows reliability results equivalent to those of the MOS capacitor, indicating that a high-quality CVD oxide can be as robust as a thermally grown oxide over n+-type diffusion.

Capacitors are used in a variety of low- and high-frequency applications ranging from power-supply bypass and decoupling to resonators, filters, and tank circuits. MIM capacitors with Q values of 90 at 2 GHz are preferred in narrow-band applications such as resonators, filters, and tank circuits, in which high Qs and low parasitic capacitance are required [40]. In contrast, PIP and MOS are typically used for power-supply bypass and decoupling. With an optimized PIP capacitor using an n+/n+ polysilicon stack, the device could have Qs approaching 30 and would be appropriate for low-frequency rf applications.

The device parameters, process, and reliability issues have been reviewed for the MOS, PIP, and MIM capacitors. The MIM has the lowest series resistance and parasitics, resulting in the highest Q of the three devices by taking advantage of low-resistivity metal plates and presence in the interconnect levels. However, a tradeoff is made, since it has a lower capacitance to compensate for its lower reliability. The MOS capacitor is on the other side of the spectrum, with high capacitance and reliability but with poor linearity and parasitics. The PIP capacitor is a higher-capacitance device; when designed over deep-trench isolation, it offers low parasitic capacitance as well. By selecting the proper dopant polarities, the linearity of the PIP can approach that of the MIM. The device has better linearity than the MOS capacitor, and if both polysilicon plates are similarly doped, very good voltage coefficients can be achieved.

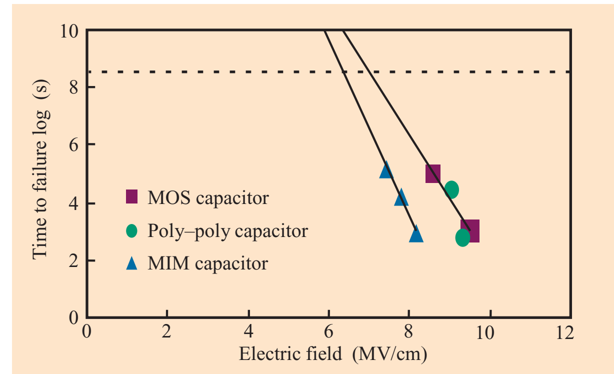

Figure 12

Time-dependent dielectric breakdown (TDDB) accelerated stress results for MOS, PIP, and MIM capacitors. Reproduced with permission from [43]; © 2001 IEEE.

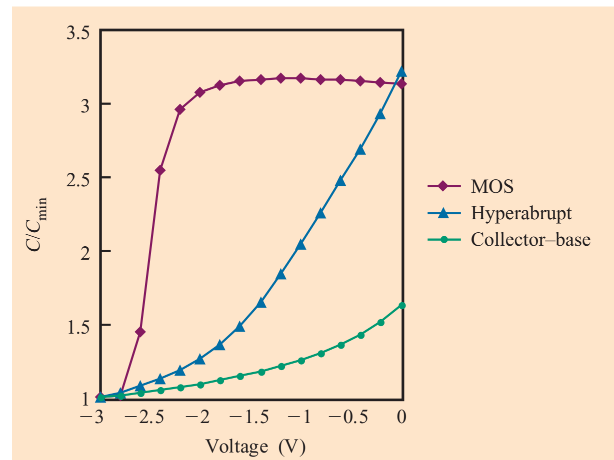

Figure 13

Normalized CV curves for hyperabrupt and MOS varactors compared to a (standard) CB junction varactor. Reproduced with permission from [41]; © 2002 IEEE.

Varactors

Varactors are essential elements of some key rf circuits, such as voltage-controlled oscillators (VCOs), phase shifters, and frequency multipliers. The key figures of merit for varactors are 1) tunability (C_{max}/C_{min}); 2) CV linearity for VCO gain variation; 3) quality factor Q; 4) tolerance; and 5) capacitance density. Traditionally, the varactor offered in BiCMOS technologies is the standard collector–base (CB) junction varactor. Three varactors have been developed for the SiGe BiCMOS and rf CMOS processes to augment this offering. These are a "quasi-hyperabrupt" enhancement of the CB diode, a MOS accumulation mode capacitor, and a CMOS diode.

Because it relies on the doping profile of the existing SiGe heterojunction bipolar transistor (HBT), the standard CB diode is not optimum for rf circuit performance. This is evidenced by a tunability of 1.7:1 between 0 and 3 V and a low degree of linearity, as shown in **Figure 13**. To overcome these problems, the quasi-hyperabrupt (HA) varactor utilizing a retrograde implant to modify the CB doping profile has been developed. To ensure independent optimization of the varactor and the HBT, an extra mask is used to introduce the retrograde

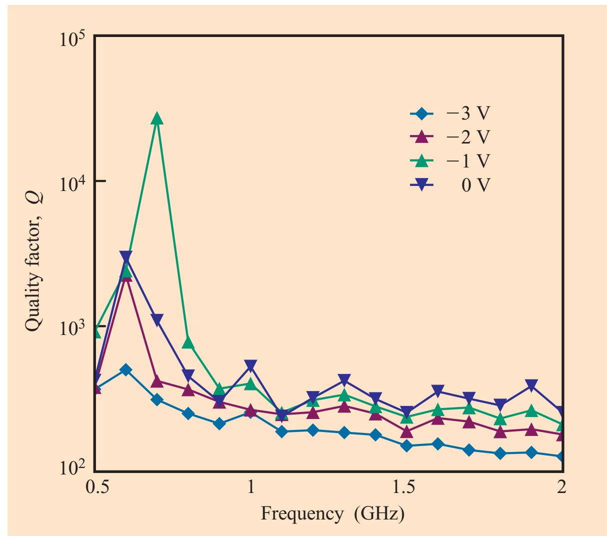

Figure 14

Quality factor Q versus frequency for hyperabrupt varactor. Q is lower for increased reverse bias as the depletion layer, and parasitic resistance, increase.

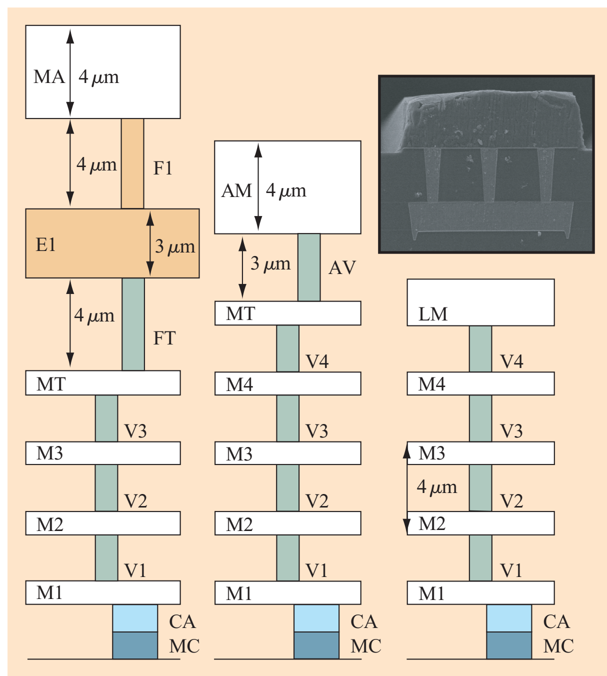

Figure 15

Schematic cross-sectional view of metallization (5HP, 5AM, 5DM). The inset shows a SEM micrograph of the top (two) thick metal layers, MA and E1 (copper), in 5DM. The thick via/metal modules in 5AM and 5DM can be added to any standard interconnect metallization.

implant. The quasi-hyperabrupt device has excellent VCO circuit performance owing to an outstanding tunability of 3.4 (0, 3 V) and a high degree of linearity, specifically in the 0-to-2-V range (see Figure 13). The extra mask is compatible with an interdigitated layout, thereby preserving the high Q of the device. **Figure 14**, which is a plot of Q as a function of frequency measured at various biases, demonstrates that the device has a Q in excess of 100 at 2 GHz.

The MOS varactor is an n-channel MOSFET fabricated in an n-well. The capacitance of this varactor is high in accumulation and decreases sharply as the device enters and goes further into depletion. This results in excellent tunability, as shown in Figure 13. The tunability is further enhanced with technology scaling, since the gate-oxide capacitance increases as the gate oxide becomes thinner. However, the MOS varactor can have lower Q because of the series resistances associated with the n-well. To maximize Q, our MOS varactor features an interdigitated layout. Interdigitating the source/drain regions minimizes the n-well series resistance, resulting in a high quality factor. The MOS varactor can be built in rf CMOS as well as BiCMOS technologies without using any extra masks.

The CMOS diode utilizes the halo typically present in state-of-the-art p-FETs to achieve the desired hyperabrupt doping profile. The varactor is basically a p+/n-well diode. The tunability is optimized by maximizing the gate-bounded perimeter and thus the overall area of the halo. The CMOS diode exhibits a tunability of about 1.7:1 over a 3-V range. This varactor can be useful for rf CMOS technologies that require better varactor linearity than a MOS varactor.

Inductors, transmission lines, and transformers

The need for high-performance passive elements in SiGe BiCMOS and rf CMOS technologies has become increasingly important recently because of the technology and integration requirements of high-functionality/low-cost rf circuit applications. On-chip passive elements, specifically monolithic spiral and multilevel spiral inductors, are a key component of these passive offerings. On-chip integration of spiral inductors poses numerous challenges. Issues related to Q, parasitics, manufacturability, design, and cost must be balanced in order to provide a competitive inductor offering [42]. For high-performance inductors, it is necessary to provide thick metallization with low via resistance for reduced series resistance [43]. The typical interconnect scaling associated with digital circuit technologies (thinning metal and dielectric levels to increase wiring density) is inconsistent with the need to keep series resistive losses low for high-quality inductors. Additionally, minimizing substrate losses due to eddy currents and capacitive coupling is desirable

in order to increase Q. Integrating the inductors in the last, thick metal levels of the BEOL and using large vias to provide a thick dielectric between the inductor and substrate helps reduce these effects [44].

Three basic metallization options are provided for spiral inductors in the IBM SiGe BiCMOS and rf CMOS technologies: a 2-μm-thick aluminum level, a 4-μm-thick aluminum level, and a dual-metal stack of 4 μm aluminum and 3 μm copper. **Figure 15** shows the integration of these levels in the BEOL. These inductor offerings have evolved over the last five years to provide high-performance inductors as rf circuit function and integration needs have evolved. Initially, the SiGe 5HP BiCMOS technology was qualified in 1998 with 2 μm Al as the last metal [45]. As can be seen from **Table 7**, this aluminum layer has a relatively high sheet resistance (14 mΩ/□); therefore, a peak Q for a 1-nH inductor at 2–4 GHz is in the range of 5 to 9. The need for higher-Q inductors drove the qualification of SiGe 5AM, an upgrade to the 5HP process with a 4-μm Al layer for improved inductor performance [2]. This layout has a 4-μm-high via below it to allow for an additional thick interlayer dielectric (ILD) between the inductor and substrate. For a 1-nH inductor, a peak Q of 18 can be realized with the 4-μm Al inductors in SiGe 5AM at a frequency of about 5 GHz. The underpass, an 0.8-μm-thick aluminum layer, has a high sheet resistance relative to the thick aluminum layer. This fixed underpass resistance shows up in series with the relatively low resistance of the 4-μm aluminum spiral metallization, limiting the achievable peak Q.

The latest IBM SiGe offering includes an additional two thick, low-resistivity metal levels above the standard BEOL stack ("dual metal"). This stack was qualified for production in November 2001. The uppermost level is thick aluminum compatible with wire bonding or C4 interconnections, with a second thick level composed of copper. Each of these levels has an additional 4 μm of oxide below it to increase the dielectric spacing from level to level and between the two levels and the substrate (see Figure 15). This high-performance offering allows not only high-Q inductors (achieved by paralleling the two thick metals for extremely low series resistance), but also high inductance density (achieved by connecting a spiral from the thick aluminum level in series with a spiral stacked below it on the thick copper level). The dual-metal inductor shown in **Figure 16** has a peak Q of 28 over a very large frequency range. Efficiently coupled structures such as transformers (impedance matching and power splitting) and baluns (balanced–unbalanced transformers used to convert differential signals to/from single-ended signals and achieved by vertically stacking windings) are also possible, with a 1:1 balun achieving a 3.5-dB untuned insertion loss. In addition to the two thick levels, an optional polysilicon shield is offered that can increase the peak Q by as much as 30% for certain geometry spirals in addition to reducing substrate noise coupling from the spiral.

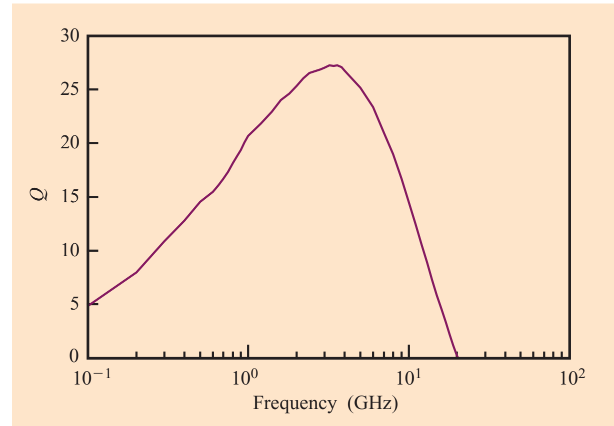

Figure 16

Plot of Q vs. frequency for a 1.1-nH dual-metal inductor. Reproduced with permission from [41]; © 2002 IEEE.

Table 7 Metal options available for fabricating high-quality passives such as inductors or transmission lines.

Metal	*Sheet resistance* (mΩ/□)	*Peak Q–* 1 nH/2–4 GHz
2 μm Al	14	5–9
4 μm Al	7	18
4 μm Al/3 μm Cu	3.2	28

The high-quality inductors achievable with the IBM dual-metal technology enable designers to integrate high-Q resonant circuits in support of low-phase-noise VCOs, narrow-band filters, low-loss-impedance matching, etc. The added ability to achieve high-quality integrated magnetically coupled structures permits the realization of on-chip baluns and transformers. Another unique advantage of using two thick metal levels with a large separation distance is the ability to create nearly ideal microstrip and/or coplanar waveguide (CPW) transmission lines with very low loss. Typical CMOS/BiCMOS/SiGe technologies are not able to achieve low-loss, ideal transmission lines because of the excessive series losses and high capacitive coupling inherent in CMOS metallization schemes.

ESD protection devices

Electrostatic discharge (ESD) protection of rf products becomes important as application frequencies exceed 1 GHz. At application frequencies below 1 GHz, the ability to simultaneously achieve excellent ESD protection and

performance objectives was possible in most CMOS, BiCMOS, and SOI applications. As semiconductor applications extend beyond 1 GHz, providing ESD protection while simultaneously satisfying performance goals, such as low capacitance on I/O pads, will increase in difficulty.

RF CMOS can utilize some of the traditional ESD solutions that are common in the industry, although many ESD solutions are unacceptable because they preclude low capacitance, high Q, and low noise. MOSFETs have significant $1/f$ noise and capacitance loading, making diode-based and diode-configured ESD implementations the preferred solutions for rf applications [46]. The integration of shallow-trench isolation (STI) has allowed for both optimization and scaling of the STI-bound p+/n-well diode, the STI-bound n+/substrate diode, and n-well-to-substrate diode structures from 0.5-μm to 0.1-μm CMOS technologies [46–49]. To maintain a constant ESD robustness in order to counter the impact of dimensional scaling from MOSFET constant electric field scaling theory, constant ESD scaling theory indicates that ESD robustness can be preserved by increasing the n-well retrograde dose with successive technology generations [46]. With the introduction of the high retrograde well dose, the p+/n-well diode capacitance can be maintained by adjustment of the n-well implant energy [46–49]. For rf technologies, the introduction of low-doped p-substrates allows for lower n+/substrate and n-well-to-substrate diode capacitance, as well as noise isolation of the ESD elements on adjacent circuitry [50–53]. RC-discriminator networks, whose RC time constant is tuned to the ESD pulse rise time, are also utilized for triggering large MOSFETs located between power supplies.

RF BiCMOS SiGe technologies offer even more opportunity to introduce low-capacitance, high-Q, low-resistance robust ESD elements for ESD protection of rf circuitry. First, for mixed-signal chips that contain digital, analog, and rf circuitry, different ESD solutions can be applied to different functional circuit blocks. The aforementioned CMOS ESD diode elements and RC-triggered MOSFET ESD power clamps can be utilized for the digital functional block. Additionally, with the myriad of additional elements offered by BiCMOS technology, new ESD elements and circuits can be utilized to provide ESD protection of digital, analog, or rf networks. This is possible by taking advantage of the SiGe library elements and the SiGe npn base, subcollector, and isolation structures. SiGe passive elements such as SiGe varactors and SiGe Schottky diodes, as well as active SiGe HBT npn devices and SiGe HBT pnp transistors, can be utilized in either diodic or bipolar configurations for networks [54–58]. Low-capacitance emitter–base and base–collector junctions provide well-controlled high-Q junctions for ESD protection networks. Low diode anode series resistance is achievable in SiGe heterojunction bipolar transistor devices because of the high base doping concentration utilized in heterojunction transistors. Heterojunctions decouple the emitter–base junction capacitance from the base doping concentration design point. For ESD structures, this allows for improved current uniformity in multi-finger base–collector diode structures. Additionally, low diode series cathode resistance, significantly lower than the CMOS well design point, is achieved using the heavily doped subcollector, reach-through, and collector implants. Additionally, removal of the Kirk-effect limiting pedestal implant lowers base–collector junction capacitance for usage of SiGe varactors in the forward-bias mode with no ESD robustness degradation. Deep-trench isolation also provides for the use of deep-trench (DT)-bound subcollector–substrate, DT-bound n-well-to-substrate, and DT-bound p+/n-well diode elements. The DT-bound structures can provide low capacitance, improved latchup immunity, and noise injection reduction, as well as higher density.

BiCMOS SiGe technology also allows for the introduction of scalable ESD power clamps for analog and rf functional blocks. To provide an ESD solution that naturally scales with the BiCMOS technology and utilizes the limitation of bipolar transistors, ESD power clamps were designed which take advantage of the Johnson limit of SiGe HBT devices [59–61]. The Johnson limit can be simply explained as the product of the breakdown voltage and cutoff frequency of a transistor being a constant, $V^*_m f_T$ = const. Thus, f_T can be traded off against breakdown voltage.

Hence, from the Johnson limit, $V^*_m f^*_T$ is associated with a first transistor, and $V_m f_T$ is associated with a second transistor. The ratio of breakdown voltages can be determined as $(V^*_m/V_m) = (f_T/f^*_T)$. Using this Johnson relationship, an ESD power clamp can be synthesized in which a trigger device with the lowest breakdown voltage can be created by using the transistor with the highest cutoff frequency (f_T), and a clamp device with the highest breakdown device will have the lowest cutoff frequency. **Figure 17(a)** shows an example of a Darlington-configured bipolar power clamp with a 47-GHz/4-V BV_{CEO} trigger device that supplies the 27-GHz/6-V BV_{CEO} clamp device. A 7-Ω ballast resistor was used for each leg of the clamp device. A 7-kΩ bias resistor was used below the trigger device to limit the current. In this power clamp, the trigger device had an open base configuration, allowing early breakdown of the trigger circuit. **Figure 17(b)** shows the human body model (HBM) ESD results. In a given BiCMOS SiGe technology, a large number of SiGe HBTs with different breakdown voltages are available to establish different trigger conditions for applications with different power supplies.

There are many advantages of the BiCMOS SiGe ESD clamp compared to RC-triggered MOSFET ESD power clamps. First, SiGe ESD power clamps provide a much higher robustness per unit micron. The RC-triggered MOSFET ESD power clamp achieves less than 2.5 V/μm, while the SiGe HBT npn achieves 15–30 V/μm of npn width. Second, the BiCMOS SiGe ESD clamp can be used for negative-power-supply voltage products. A disadvantage of the MOSFET RC-triggered clamp in a single- or dual-well technology is that it cannot be used between V_{DD} and negative-power-supply V_{EE} because of MOSFET overstress. Third, in contrast to MOSFET ESD networks, the ESD robustness per unit micron (width) does not decrease with successive rf technology generations. Experimental results from three successive SiGe technologies do not show degradation of ESD robustness.

To evaluate the ESD scaling of a SiGe HBT device, a dimensionless group can be established explaining the relationships among thermal conduction, thermal capacity, failure temperature, pulse width, saturation velocity, maximum electric field condition, and the unity current gain cutoff frequency [52, 62–64]. This analysis shows that the frequency of the SiGe HBT increases as the maximum power decreases. As the device dimensions are scaled to achieve these objectives, the power at which failure occurs will decrease unless doping and material changes are addressed. To produce future high-f_T devices, dimensional scaling, doping concentration, and material changes will be needed. This will entail optimization of concentrations of the base dopant, Ge, and carbon. In the evolution of these HBT devices, the choices made to achieve the BV_{CEO} and the f_T will influence both the maximum power and ESD robustness.

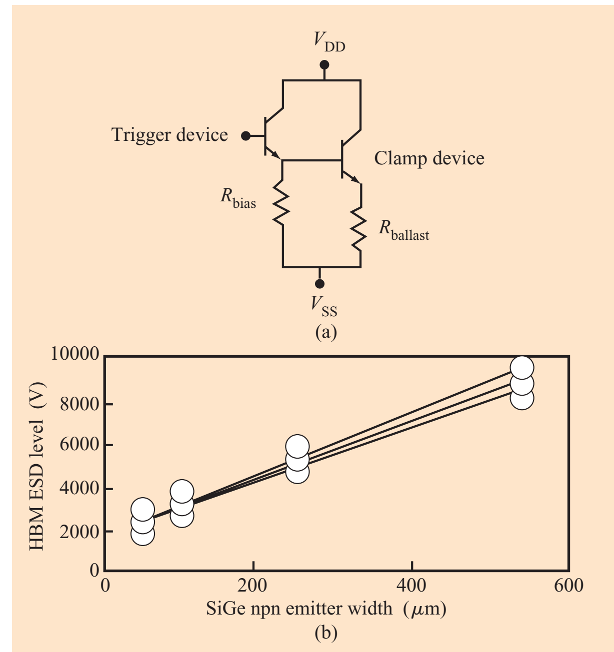

Figure 17

(a) SiGe HBT ESD power clamp utilizing a high-f_T/low-BV_{CEO} trigger element and a low-f_T/high-BV_{CEO} clamp element. The ballast and bias resistors are 7 Ω and 7 kΩ, respectively. (b) Human body model (HBM) ESD robustness as a function of SiGe HBT power clamp emitter width. Reproduced with permission from [59]; © 2001 IEEE.

3. Communications technology design and process development

Technology design

Although Si/SiGe HBT devices have been proposed for many years, the first practical SiGe devices were fabricated in IBM in the late 1980s, in large part enabled by the development of the ability to grow Si/Ge epitaxial layers at low temperatures using ultrahigh-vacuum chemical vapor deposition (UHV/CVD) [65]. This technique freed device designers to be able to grow arbitrary doping profiles without the constraints of high thermal cycles previously thought necessary for the creation of perfectly crystalline material. This activity has led to substantial improvements in the SiGe HBT over several generations by careful scaling of the epitaxial transistor (ETX) device [66] with changes in the low-temperature epitaxy (LTE) base region through modifications in Ge ramp, boron profile, collector design, and carbon doping.

Decisions for the development of new technologies are initiated by marketplace and circuit design requirements, which in turn determine the choice of a BiCMOS technology. While HBT performance (f_T, f_{max}, and I_C at peak f_T) is frequently of prime importance for these decisions, attention must be paid to CMOS generation (performance, density, V_{CC}, ASIC compatibility), passive elements, and current-carrying capability. Further restrictions may be placed on a technology by cost and reliability needs. These technology requirements are generated primarily by the marketplace and individual customer strategy. The IBM technology design methodology has been to drive continuous improvement in performance of HBT, CMOS, interconnection technology, and passive elements. Exploitation of all of these enhancements simultaneously, generally introduced into the IBM SiGe high-performance (HP) technologies, increases process complexity and mask count and, therefore, cost. While this is necessary for a large segment of the BiCMOS marketplace, smaller individual markets can be satisfied with reduced technology features through careful development of analog derivative technologies at a reduced cost.

With improvements in both CMOS performance and passive elements, a major market for rf CMOS is also emerging, with new issues which must be addressed. Smaller chip sizes, a pad-limited total chip area, and the predominance of passive components are layout issues that generally distinguish analog and rf designs from their digital counterparts. At the same time, passive device area and wire-bond pads have not decreased with the reduced lithography dimensions; chip areas remain roughly the same for a given function, even with improved lithography dimensions. Consequently, the economic forces driving reduced lithography in digital CMOS technologies (that is, the tradeoff between the lithography-driven chip cost increase and the ability to obtain more chips on a wafer or more functionality per chip) do not apply in the analog and rf domain.

Digital CMOS trends do not influence analog designs. They are costly, and in many cases digital CMOS changes make analog designs significantly more difficult. For example, metallization trends toward thinner films result in higher inter- and intra-level capacitance (per unit area), thereby compromising the performance of designs that retain device-to-device distances between technology generations. These manufacturing limitations are in addition to analog circuit requirements that make it more difficult to design with reduced supply voltages. The net result from this "nonscaling" is that, when compared to digital CMOS, analog and rf technology roadmaps are less defined. Market and targeted design understanding are critical to defining the best mix of technology elements and dimensions.

Process integration

IBM has demonstrated leadership in the development of world-class analog bipolar and BiCMOS process technologies since its introduction of the world's first SiGe bipolar technology, SiGe 5E, into production in 1996 [67]. Although this premier technology, intended for early fabrication of wireless circuits, did not include all CMOS elements, subsequent high-performance (SiGe HP) technologies have all been fully compatible with corresponding ASIC CMOS technology, resulting in the ability to integrate large amounts of both high-performance analog and digital signal processing. The evolution of these SiGe production technologies spanning 0.5-μm, 0.25-μm, and 0.18-μm generations has been through a combination of vertical scaling (improved SiGe epitaxial films and bipolar profiles), horizontal scaling (improved lithography dimensions and overlay), and CMOS innovation (gate lengths, density, and metallization technology). The improvements in SiGe HP technology are illustrated in Figure 21 (shown later). Details of these technologies demonstrate that the primary technological driver in going from SiGe 5HP [68] to 6HP [2] was improvement in CMOS, while the migration to 7HP [3] was driven by bipolar performance and included the addition of Cu BEOL and further substantial improvements in CMOS.

Semiconductor innovations have been introduced into each successive technology in order to meet the requirements of the marketplace for the rapidly growing wireless industry and the need for higher-bandwidth optical networking products. The development of an integrated SiGe BiCMOS technology originates with an understanding of semiconductor requirements imposed by the marketplace. The wireless customer envisioned for SiGe 5HP could be serviced with a cost-competitive CMOS technology (ASIC CMOS 5X) and analog capabilities achieved with a 50-GHz HBT capable of driving speeds for applications in the 2–5-GHz range. HBT and CMOS technologies were successfully merged by sharing a common polysilicon film for both bipolar extrinsic base and CMOS gate structures. This integration method, referred to as *base-during-gate* (**Figure 18**), allowed cost-efficient use of films and masking levels and was made possible by the thermal compatibility of early CMOS structures with the rather deep emitter profile developed in the early HBT. It was clear that Ge doping profiles had a profound effect on both HBT performance and strain that could result in decreased circuit yields, so Ge doping was intentionally kept low to facilitate early production learning. Acceptability by the analog marketplace also required the addition of the high-quality passive elements (resistors, capacitors, inductors, etc.) discussed in detail in the preceding section.

SiGe 6HP was developed first for applications used in storage products which require a very large circuit count of high-performance CMOS such as the read-channel chip described in the next section. For these applications, it was necessary to replace the 0.5-μm CMOS of SiGe 5HP with the 0.25-μm CMOS 6SF. The reduced thermal cycle used in this CMOS generation also required a modification of the integration from base-during-gate to an integration methodology, which fabricated the critical emitter–base region of the HBT after CMOS structures were in place [Figure 18(b)]. While this integration requires careful protection of the CMOS gate conductor during the processing of the HBT, and subsequent removal of these protective films, this base-after-gate integration was successful in the decoupling of thermal cycles required for narrow HBT profiles and the CMOS device activation.

While the first two generations of SiGe BiCMOS could successfully service applications up to 10 Gb/s (OC-192 SONET), 40-Gb/s (OC-768) optical networking products require a substantially faster bipolar transistor. SiGe 7HP was developed for this high-switching-speed-driven application space. Since designers request bipolar devices

that switch at approximately three times the bit rate of multiplexing and demultiplexing circuits, the SiGe 7HP target was established at a maximum oscillation frequency of 120 GHz. To successfully achieve these speeds, previously widely believed to be achievable only with III–V compound semiconductors (notably InP-based HBTs), vertical scaling (reduction of epi base and collector profiles) as well as horizontal scaling of the HBT device was necessary. The reduction of vertical profiles necessitated careful control of process thermal cycles as well as the use of carbon doping [69], which had not been necessary in the early generations of IBM SiGe BiCMOS. In addition to continued improvements in passives, the integration of this technology with CMOS 7SF (0.18-μm gate length) marked the introduction of Cu interconnection technology, which further enhanced the current-carrying capability of high-performance circuits.

The self-aligned HBT transistor utilized in generations 5HP, 6HP, and 7HP required evolutionary modifications of the ETX transistor [66], which featured the ion implantation of the heavily doped extrinsic base region of the device. Further scaling of the ETX device would require extensive reduction in intrinsic base doping. This would lead to high pinch base sheet resistance, which would lead to a non-optimal design point for a technology based on high manufacturability. Necessary improvements to ETX in base resistance (and collector–base capacitance), which determined the maximum available power gain frequency, f_{max}, were limited by this device structure. This shortcoming therefore led to the development of a new integration scheme. The raised extrinsic base (RXB) bipolar was introduced to allow further vertical and horizontal scaling without the limitations imposed by the ETX device. By contacting the lightly doped intrinsic base with an additional boron-doped polysilicon film, these constraints were lifted, and the HBT introduced for SiGe 8HP integration has demonstrated f_T and f_{max} values in excess of 200 GHz.[5]

In addition to the flagship 5HP, 6HP, and 7HP SiGe technologies, several derivative SiGe technologies have been developed to capture smaller markets with more specific requirements. These derivative technologies include SiGe 5PA, SiGe 5MR, and BiCMOS 5HPE, which are targeted respectively at rf power amplifier, disk drive preamplifier, and wireless applications.

The SiGe 5PA technology was developed as a derivative of the SiGe 5HP technology targeted at the rf power amplifier market. Power amplifiers for wireless handsets have historically been built using GaAs because of its ability to achieve the competing breakdown and linearity requirements that were previously unattainable with silicon technologies. SiGe 5PA meets these requirements

[5] B. Jagannathan, unpublished communication.

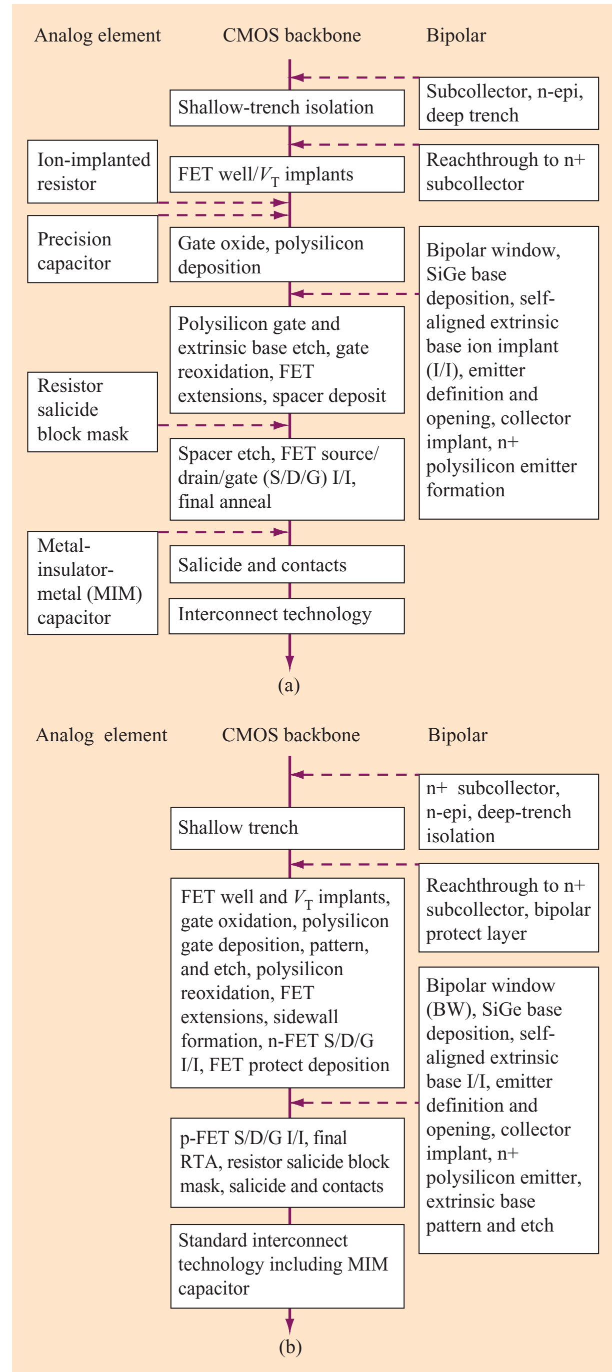

Figure 18

Schematic process flow diagram for (a) 0.5-μm base-during-gate (BDGate) production technology. (b) 0.25-μm and 0.18-μm base-after-gate (BAGate) production technology. Note the reduced number of analog and bipolar blocks compared to the BDGate process, because the CMOS now contains many analog modules. (For both cases, the CMOS backbone represents the base CMOS process. Insertion points are shown for analog and bipolar process modules.) Reproduced with permission from [2] and [44]; © 1999 and 2001 IEEE.

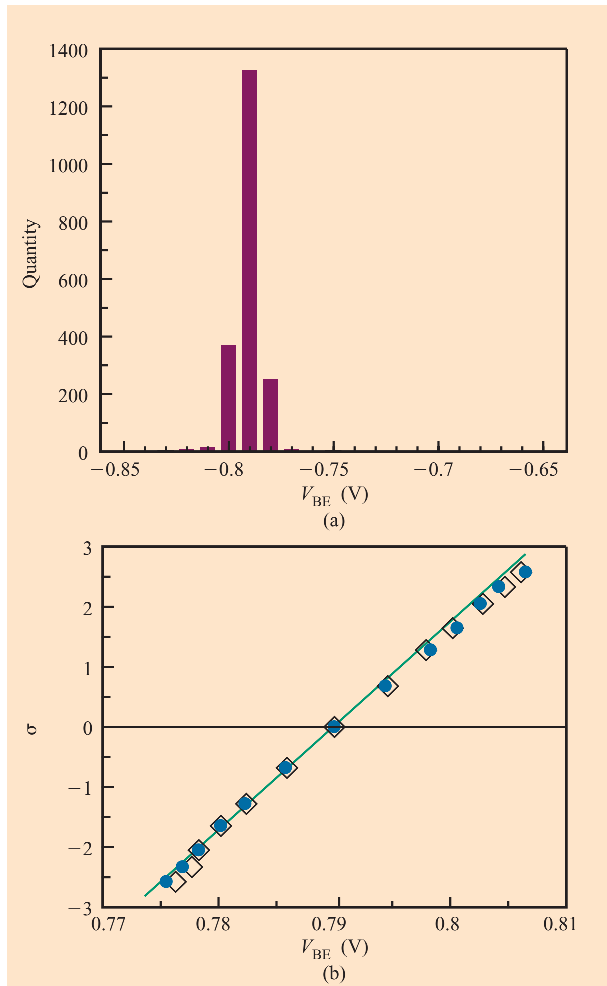

Figure 19

Example of statistical device models showing (a) histogram of V_{BE} for 0.5-μm × 1.0 μm HBT at 10 μA emitter current; (b) probability plot for V_{BE} comparing measured hardware (diamonds) on approximately 2000 samples and device model (circles) to a normal distribution (curve). Reproduced with permission from [45]; © 1997 IEEE.

with a high-breakdown SiGe HBT that has a BV_{CEO} of 7 V and a BV_{CBO} of 20 V. The increased breakdown voltages are achieved, while minimizing the impact to the device linearity and f_T, through modification and optimization of the collector doping profile. The technology is defined such that the remaining device set is common with those in the parent SiGe 5HP technology.

The SiGe 5MR technology was developed for disk drive preamplifier applications, which have a conflicting combination of performance and voltage technology requirements between the read and write portions of the chips. The read-amplifier portion of the chip must amplify extremely small signals from the magnetoresistive read element while not significantly degrading the signal-to-noise ratio (SNR). Conversely, the write portion of the chip requires high-voltage devices to drive high-speed signals through the inductive write head. The SiGe 5MR technology includes a SiGe HBT capable of achieving the performance and noise requirements of the read amplifier, yet having a BV_{CEO} of 10 V to support the voltage requirements of driving the inductive write head. The CMOS devices included in the technology for logic control circuitry support the industry-standard disk drive supply voltage of 5 V. The technology was developed by combining the 5-V CMOS devices from CMOS 5SF, the proven SiGe HBT from SiGe 5HP, breakdown voltage enhancements similar to SiGe 5PA, and the base-after-gate integration scheme from BiCMOS 6HP. Additional development efforts focused on adding features such as a lateral pnp, an isolated n-FET, and a polysilicon–polysilicon capacitor, as well as process simplifications targeted at cost and cycle-time reduction.

These features of the SiGe 5MR technology are all key elements included in its derivative technology, BiCMOS 5HPE [70]. The combination of a rich feature set and simplified process provided by this technology makes it well suited for the competitive wireless marketplace. The BiCMOS 5HPE technology includes the features of SiGe 5MR, together with an additional higher-performance SiGe HBT and enhanced passives such as the 1.35-fF/μm^2 MIM, high-Q inductors, and MOS varactor. Process simplifications such as replacing long furnace anneals with rapid thermal anneals (RTAs) significantly reduce the production cycle time. This cycle-time reduction is extremely valuable for wireless product developers who depend on multiple design passes to debug sensitive rf circuits.

Manufacturing issues

To introduce semiconductor technology into a production environment, it is necessary to demonstrate a rigorous set of manufacturability standards. These requirements can be loosely categorized as repeatability, reliability, and yield. Device models are developed to describe devices fabricated using a large statistical database collected on a substantial quantity (typically 100–300) of wafers fabricated during this assessment. These models begin by analysis of device parameters, as illustrated in **Figure 19**. The models describe nominal values and distributions of manufactured devices from probability plots. Similar data is collected on in-line measurements of physical parameters such as lithographic critical dimensions and overlay, film thicknesses, and layer resistances and physical properties. Both device electrical data measured on test structures and in-line parametric measurements are collected during the qualification in order to demonstrate statistical process control (SPC) [71]. SPC methods compare measured data to well-defined process

specifications and must meet rigorous standards in order to proceed with volume production. SPC measurements of Cp (a gauge of process centering) and Cpk (process capability index) are illustrated in **Figure 20**. A Cpk value of 1.0 represents the point at which 3σ of the population distribution is within the specified manufacturing control limits, with values in excess of 1.0 indicative of much tighter production control.

SiGe HBT reliability stressing is conducted in both forward-bias and reverse-bias modes, using the same accelerating stress conditions and analysis techniques developed for previous implanted-base silicon bipolar technologies [72]. In forward bias, less than 5% change in npn current gain β over a 500-hour stress at 140°C and 1.3 mA/μm^2 (near peak f_T) was found for the 0.5-μm-generation SiGe HBTs. Most GaAs HBT technologies are stressed at currents far less than their peak f_T current [73], which does not represent realistic use conditions. Using empirically determined acceleration factors, the SiGe HBT forward-bias result is equivalent to less than 10% β degradation under typical-use conditions (1.25 mA/μm^2 at 100°C) after 100000 power-on-hours (POH). Change in β has been attributed to electromigration-induced pressure on the emitter contact, causing decreased collector current with stress condition [74]. Reliability at high current densities with SiGe 7HP and 8HP vertical scaling also requires a careful look at the choice of interconnection technology and device self-heating considerations [75]. With reverse bias of 2.0 V or less, no measurable change in base or collector currents is observed at a worst-case condition of −40°C. Hot-electron degradation with reverse bias stress is also typical of bipolar junction transistors and is substantially lower for the epitaxial (epi)-base devices when compared to ion-implanted base double polysilicon [74]. This result is attributed to the reduction of the electric field at the emitter–base junction due to a base doping setback which can be achieved with epitaxial base growth and is expected to be similar with HBT vertical and horizontal scaling.

A major focus for final production qualification decisions is the capability of a technology to achieve high manufacturing yields. FET yield assessment and control in SiGe BiCMOS technologies is adopted from the parent CMOS technologies, with an added focus on ensuring that the SiGe process steps do not degrade the FET yield. For example, with the base-after-gate integration scheme, several bipolar films are deposited over the FETs and then subsequently etched away. Defect-free removal of these films over the FET regions is critical to minimize yield loss due to shorting. Successful removal of the bipolar films from the FET regions is monitored with both large-area defect monitors and CMOS SRAM yields. A BiCMOS 6HP 30-lot yield trend for large-area monitor structures [2] demonstrates that BiCMOS yields are equivalent to the typical yield of the parent CMOS technology. CMOS SRAM yields were also shown to be within the parent CMOS target range, as indicated by the BiCMOS 6HP CMOS SRAM yield trend shown in **Figure 21**.

Silicon bipolar transistor device yield has historically been limited by dislocations in the silicon crystal that cause junction shorting [76]. One would expect SiGe HBTs to have a higher density of these dislocations because of defect formation during epi growth and strain in the Ge layer. However, the low-temperature epitaxy (LTE) process technology produces a relatively defect-free epi layer and does not significantly contribute to yield loss. Also, minimizing the post-epi growth during thermal

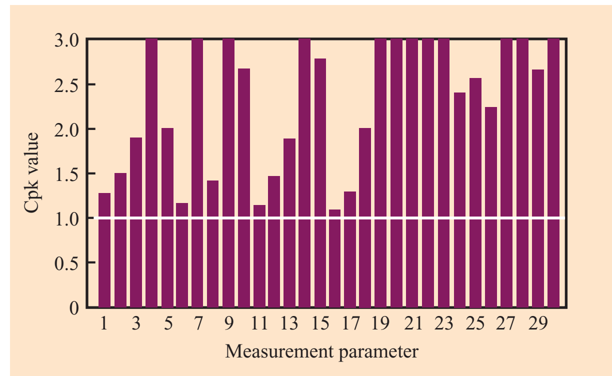

Figure 20

Statistical process control chart showing achievement of good process control over a wide range of in-line process measurements. Values of the process capability index (Cpk) of 1.0 indicate process measurements at the 3σ control point. Values of 1.5 are considered under 6σ control.

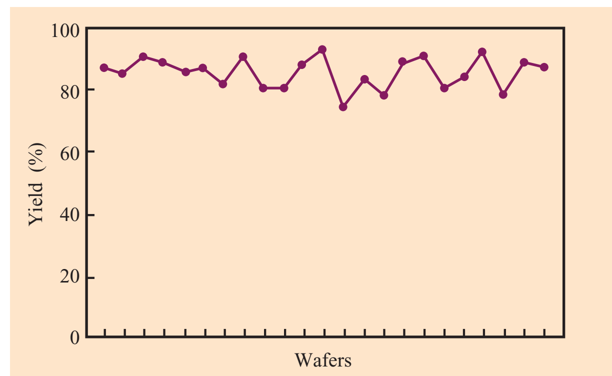

Figure 21

Static RAM functional perfect (zero bit fails) yield data from a 154K RAM (12-μm^2 cell size, one million FETs) by wafer. Reproduced with permission from [2]; © 1999 IEEE.

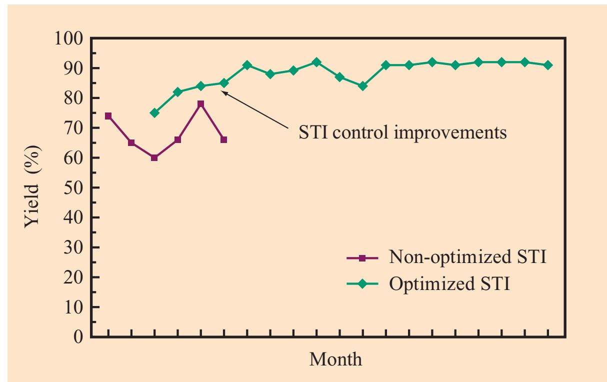

Figure 22

Example of yield learning showing HBT yield improvement over time through modification of process controls. Copyright Canon Communications LLC. Used by permission.

cycles helps reduce the possibility of forming defects due to the strained layer. The primary cause for defect generation has been found to be related to stress due to shallow-trench isolation (STI). As a result, the STI formation process has been optimized in order to minimize the stress and increase the HBT yield. **Figure 22** shows a SiGe 5HP 20-month all-good-yield trend of an array of 4000 HBTs. Initially, the yield was depressed, averaging in the 60–70% range. Through careful optimization of the HBT process, the yield has been improved substantially, to above 90% [77].

The real test for the success of a SiGe BiCMOS technology was being able to design and manufacture highly integrated products with good yields. An example of an integrated circuit that was produced in high volume at the IBM Essex Junction facility is a read-channel chip that translates analog signals from a disk-drive read head into digital words. The analog data is interpreted using a partial response maximum likelihood (PRML) signal processing algorithm. The chip was clocked at a rate of 75 MB/s, which was the fastest PRML chip speed published at that time.

4. Technology implications in design

Device noise and isolation issues

Noise plays a pivotal role in the design of both wireless and wired communications systems. In a wireless system, for example, data is carried by a signal that resides over a specified bandwidth and assigned frequency. In-band noise added to the signal by the transmitter circuits during travel through the free-air channel and noise within the circuits of the receiver combine to decrease the SNR. Together with the available bandwidth, this SNR has a direct impact on the data rate that the system can achieve for a given bit-error rate. While the SNR can be improved by increasing the transmitted power or decreasing the transmission distance, such strategies trade off directly against the market trend for increased range, portability, and battery life. Noise is a key limiting factor in the performance of optical networking systems as well, particularly with data rates now exceeding 40 Gb/s. Such high rates compress each data symbol into an extremely small interval of time and require precise timing to detect. Any noise or jitter in this timing, such as from phase noise in the circuits that generate the clock signal, can result in a detection error.

Noise may be introduced into a signal in a variety of ways. One source is the set of devices, both active and passive, comprising the circuits of the transmitter and receiver chips. In a technology capable of system-level integration, however, noise may also be introduced when one circuit injects an unwanted signal into another circuit on the same chip, either through the air or the substrate. Understanding each of these various noise properties is essential for the optimal design of low-power, high-data-rate communications chips. The IBM SiGe BiCMOS technologies each feature a device library containing a wide variety of bipolar, FET, and passive devices. In developing a circuit, a designer selects one device over another based on relative merits, including the expected noise performance of a circuit employing that device. Several figures of merit are used, depending on the circuit application.

One of the most common circuits in analog and rf design is the amplifier. In a wireless receiver, for example, the signal present at the antenna is often very weak. This signal is first narrow-band filtered to eliminate all out-of-channel energy, including noise, before passing through a low-noise amplifier (LNA) designed to increase the signal level significantly while introducing as little noise as possible. In this class of circuits, the noise property of greatest interest is how the SNR of the narrow-band signal at the channel frequency is degraded from input to output. This property may be captured through a figure of merit known as the noise figure, which is defined simply as the input SNR divided by the output SNR at a given temperature. The noise figure may be measured between the input and output of an individual active device as well. An ideal, noise-free device displays a noise figure of 1 (or 0 dB, as it is most commonly expressed), while the noise figure of a physical device is higher. Since the noise figure depends on the impedance of the input source, the device under test is commonly measured over a variety of source tunings in order to find the state (typically stated as reflection coefficient, Γ_{opt}) that achieves the minimum noise figure value (F_{min}). The power gain (G_A) associated with this tuning state can be noted as well.

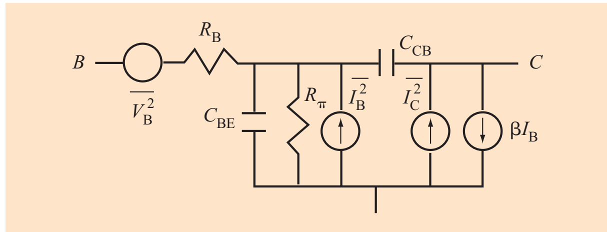

Figure 23

Simplified equivalent circuit noise model for a bipolar transistor.

In a BiCMOS technology, designers have the option of using bipolar or FET transistors as active devices in analog and rf circuits. The SiGe bipolar device features several intrinsic properties that make it particularly attractive for low-noise circuits such as LNAs. These properties can be understood in terms of the simplified bipolar equivalent circuit noise model illustrated in **Figure 23**. The model focuses on the three sources of noise that dominate in a typical modern device.

The first source is thermal noise generated in proportion to the temperature and value of the base resistance, R_B, and the design of the SiGe bipolar achieves a low value for this resistance. Germanium narrows the bandgap of the base with respect to the emitter, decreasing the amount of hole injection into the emitter for a given electron injection into the base. This effect compensates for the loss of β that would otherwise occur with high base doping, allowing a reduction in the sheet resistance of the intrinsic base. Further, the lateral distance that base current must travel through the intrinsic base from edge to center can be made quite small through the use of advanced lithography to define a very narrow emitter stripe width. Such a narrow width is made possible by a polysilicon emitter construction that achieves uniform dopant distribution even at dimensions of 0.1 μm.

A second source of high-frequency noise in the bipolar transistor is the fundamental operation of the emitter–base p–n junction itself, which contributes shot noise in proportion to both the base (I_B) and collector (I_C) currents. The SiGe bipolar device keeps these noise components under control by two means. The high β created by the presence of Ge in the base keeps I_B low for any given I_C bias, reducing I_B shot noise. Further, the low parasitic resistances and capacitances that contribute to high f_{max} (e.g., R_B and C_{CB}) result in high power gain at typical frequencies of interest. This high gain allows an input signal to be amplified to much larger levels before the addition of shot noise, reducing the impact of this shot noise on the output SNR and thus improving the noise figure.

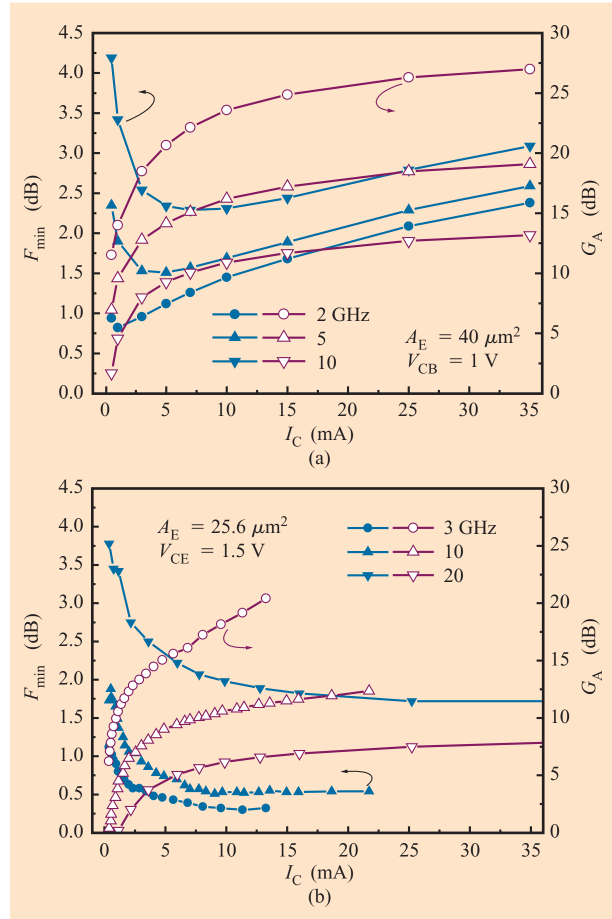

Figure 24

Minimum noise figure and associated gain for a 0.5-μm-generation SiGe bipolar transistor with an emitter area of 40 μm^2, measured at 2, 5, and 10 GHz (V_{CB} = 1 V). (b) Minimum noise figure and associated gain for an 0.18-μm-generation SiGe bipolar transistor with an emitter area of 25.6 μm^2 measured at 3, 10, and 20 GHz (V_{CE} = 1.5 V). Reproduced with permission from [7]; © 2001 IEEE.

Although these generic SiGe bipolar features favor a low noise figure for any given generation, there is also a generation-to-generation scaling trend toward a lower noise figure. This improvement results from distinct lateral and vertical scaling trends in device design. Lateral scaling reduces R_B and improves gain by reducing parasitic capacitances. Vertical scaling leads to reductions in transit time that further improve power gain. Both R_B and gain may also improve as a result of fundamental changes in device architecture aimed at reducing parasitics.

Figure 24(a) displays both the minimum noise figure, F_{min}, and associated gain G_A as a function of I_C for a 0.5-μm-generation (45-GHz f_T, 65-GHz f_{max}) device with an emitter area (A_E) of 40 μm^2. The 0.5-μm technologies,

including IBM SiGe 5HP and 5AM, are the generations most widely used at present for 1–5-GHz wireless telephony and data networking because of the attractive cost–performance balance. The figure shows data for two frequency bands. At 2 GHz, near the band used by several standards of wireless telephony, we observe that the device achieves a minimum noise figure of 0.8 dB at a current of 1 mA. At the higher bias of 5 mA, the device maintains F_{min} below 1 dB, with an increased associated gain of 20 dB. At 5 GHz, a band used for high-bit-rate wireless data networking, F_{min} remains below 1.5 dB, with an associated gain of 14.2 dB at the same 5-mA bias. While there are no high-volume wireless applications in the 10-GHz regime at the moment, we note that an IBM device shows F_{min} of about 2.3 dB in this band, with associated gains of 10–12 dB. As we note below, a 40-μm^2 device area is non-optimal for 10-GHz operation owing to source-matching difficulties. Indeed, smaller devices (e.g., $A_E = 2.5\ \mu m^2$) have demonstrated 10-GHz F_{min} values of $<$1.8 dB.

High-frequency noise performance improves on moving to the 0.25-μm SiGe BiCMOS generation (e.g., 6HP). While the basic structure of the 0.25-μm bipolar is similar to that of the 0.5-μm generation, the lithographic improvements allow for a somewhat narrower emitter stripe, achieving a reduced R_B. The result is an improvement in F_{min} of about 0.1 dB in the 1–10-GHz span. Combined with the ability to integrate a more aggressive CMOS, this generation is also attractive for use in the 1–5-GHz band, while adding the ability to mix analog/rf circuits with large gate counts of high-speed logic.

Both the 0.5-μm and 0.25-μm SiGe generations offer a high-breakdown voltage variant of the bipolar transistor, featuring a modified collector profile that also results in reduced R_B and C_{CB}. Although this transistor suffers f_T falloff from the Kirk effect at much lower current densities compared with the high-f_T variant, this current threshold is much higher than the biases resulting in best noise performance and is thus not a limitation. A designer can achieve an additional improvement in F_{min} of about 0.1 dB by using this device, although the poorer linearity characteristics of the device may limit suitability for many applications.

Although the first applications of the 0.18-μm-generation SiGe BiCMOS technology, known as 7HP, have been 40-Gb/s optical networking, the technology also represents a significant improvement in noise performance and may therefore be attractive for wireless design as well. The benefits result from both lateral and vertical scaling, which improve R_B, β, and power gain in the device. The improvements in gain are particularly important for reducing the noise figure at higher frequencies (e.g., 10 GHz and above). As an example, **Figure 24(b)** illustrates F_{min} and G_A behavior vs. I_C for a 25.6-μm^2 device at 3, 10, and 20 GHz. The 3-GHz band is close to the unlicensed 2.4-GHz band commonly used for wireless data networking. At this frequency, the 7HP device achieves an F_{min} value of only 0.4 dB and maintains this value for associated gains exceeding 20 dB. At 10 GHz, F_{min} climbs to only 0.6 dB, demonstrating the possibly greater suitability of the 0.18-μm generation for higher-frequency wireless work compared to 0.5 μm and 0.25 μm. Associated gains exceed 12 dB. Further, F_{min} values of 1.7 dB are achievable out to 20 GHz, approximately double the frequency of the earlier generations for equivalent performance and consistent with the 2.5× (1.5×) increase in f_T (f_{max}).

Tuning for a desired combination of noise figure and associated gain requires a designer to create a network to match the source impedance (typically 50 Ω) to the optimum noise impedance of the device. This task is greatly simplified if the real part of the desired match is already 50 Ω, allowing the imaginary part to be matched with a simple inductor in series with the base. This condition may be realized by scaling the device area appropriately. For example, for a 0.5-μm-generation, 40-μm^2 bipolar transistor biased at an I_C of 5 mA, F_{min} at 2 GHz is achieved at a matching impedance of (68 + j37) Ω. Scaling the device up to the slightly larger area of 54 μm^2 would achieve the desired 50-Ω real match, requiring an approximately 3-nH series inductor to complete to match. In comparison, a 0.18-μm-generation, 25.6-μm^2 bipolar biased at 10 mA achieves an optimal match at 10 GHz with a source impedance of (7.7 + j13.6) Ω, pointing out the need to scale the device down to a more suitable emitter area of 3.9 μm^2.

High-frequency, or broadband, noise is not the only category of noise pertinent to analog and rf design. In addition to low-defect-density single-crystal silicon, the structures of both bipolar and FET transistors contain a number of interfaces to surface films, particularly to SiO_2. These interfaces contain a relatively large number of defects which act as electron and hole traps. The exchange of carriers between these traps and the active regions of the device leads to the phenomenon of 1/*f* noise. This mechanism manifests as a high noise energy content near dc, tapering off with frequency approximately as $(1/f)^n$ before merging with the broadband noise spectrum at a higher frequency approximated by a figure of merit known as the corner frequency. As initially introduced into the signal by the device, this low-frequency noise is generally out of band. However, subsequent signal processing by a mixer can shift the noise spectrum to straddle the carrier frequency, potentially causing jitter as well as interfering with adjacent channels. Thus, designers will seek a device with good 1/*f* noise properties when creating circuits such as LNAs and VCOs that eventually send their output to a mixer.

Bipolar and FET devices differ greatly in their $1/f$ noise properties. Because the electrical characteristics of the bipolar transistor are determined by mechanisms that occur below the surface of a silicon substrate, away from oxide interfaces, these devices show significantly better $1/f$ noise results than FETs. Indeed, generation-to-generation scaling in FETs moves oxide interfaces even closer to the active channel, resulting in worsening of $1/f$ performance. The bipolar device is largely immune from this, maintaining a low corner frequency across generations.

Figure 25 compares the $1/f$ performance of four devices from the 0.18-μm SiGe 7HP BiCMOS technology: a 3.3-V n-FET, a 3.3-V p-FET, a high-f_T SiGe bipolar, and a high-breakdown SiGe bipolar. We focus on the 3.3-V FET variants here, since these devices support the higher supply voltages commonly used to achieve signal headroom[6] in analog circuit design. The proximity of surfaces contributes significant noise signal in the n-FET, extending out well beyond 100 kHz. The p-FET is an order of magnitude better, partly owing to the lower drain current of the p-FET at the same gate bias.

Compared with both FETs, the SiGe bipolar transistor shows significantly better $1/f$ noise performance, with an output noise signal that is lower than with an n-FET by a factor of 50 and with a resulting corner frequency of less than 1 kHz. This bipolar $1/f$ noise performance is similar to that achieved by prior generations, emphasizing the device tolerance to scaling. The modified collector profile of the high-breakdown bipolar results in reduced avalanche current even below breakdown, resulting in yet lower noise at higher frequencies compared with the high-f_T variant.

A key advantage of a high-performance BiCMOS technology is the ability to create a wide variety of circuit types integrated together on the same chip to form a complete system. One consequence of this integration, however, is that signal from one circuit can couple inadvertently into another circuit, particularly through the substrate. For example, these extraneous signals may consist of digital switching noise from a logic block or a strong, information-containing signal such as the output of a power amplifier. In any case, the coupled signal is undesirable and is thus another form of noise. To control this coupling, a designer may employ any of a number of isolation techniques drawn from among the structures available within the technology being used.

Achieving good isolation is a two-step process. The first line of defense is to prevent extraneous signal from entering the substrate in the first place. This is easiest when the signal is being injected capacitively from metal-level structures above the substrate, such as interconnects, lower MIM capacitor plates, and inductor coils. The substrate may be shielded from such signals through the use of ground planes placed beneath the injecting metal structures. In the IBM SiGe BiCMOS family, a number of technology elements may be used to construct a ground plane, including a lower level of metal such as metal 1, the FET gate or resistor polysilicon, or the bipolar n+ buried subcollector. Coupling may also be reduced by effectively increasing the distance between the injecting metal and the substrate through the use of a crosshatched mesh of deep-trench structures, which consist of 6–7-μm physical trenches lined with oxide and filled with polysilicon.

The substrate cannot always be shielded from stray signals, however. Such is the case with signals generated by the active devices themselves, which reside in the substrate. The collector of a bipolar transistor or the drain of a FET is strongly capacitively coupled to the substrate through a p–n junction and is potentially capable of injecting carriers into the substrate that may travel to and be detected by circuits elsewhere on the chip. To isolate circuits from this type of coupling, a designer may surround either the injecting or noise-sensitive circuit (or both) with a structure designed either to block the flow of the injected carriers or to collect these carriers and shunt them safely to ground. One such structure is the deep trench. Another is an ohmic substrate contact in the form of a p+ implant connected to ground. Either structure may be formed into a protective, isolating moat.

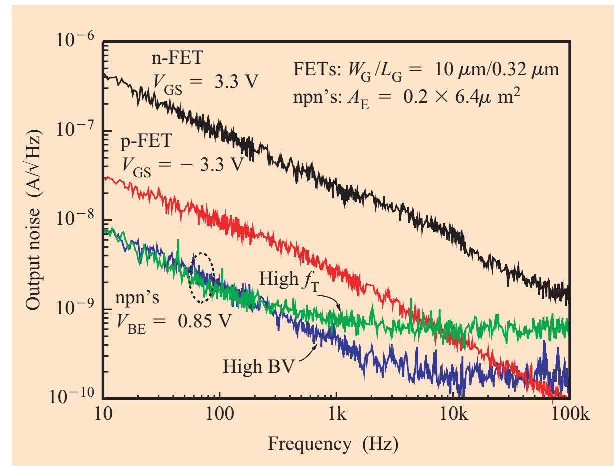

Figure 25

$1/f$ output noise vs. frequency for 3.3-V n-FET, 3.3-V p-FET, high-f_T SiGe bipolar, and high-breakdown SiGe bipolar.

[6] The term *headroom* denotes the processing power beyond that required by the application.

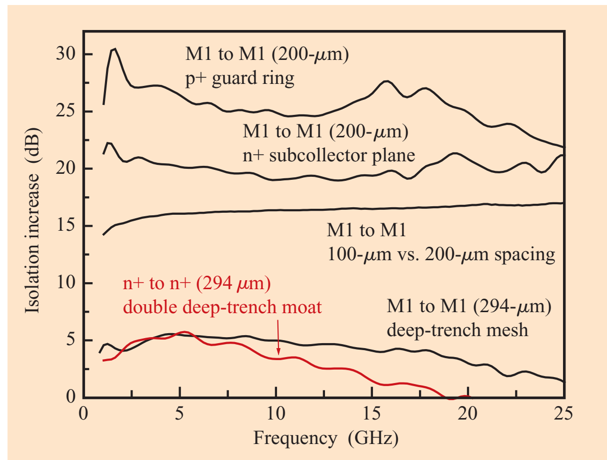

Figure 26

Isolation increase vs. frequency for a variety of isolation schemes. Reproduced with permission from [7]; © 2001 IEEE.

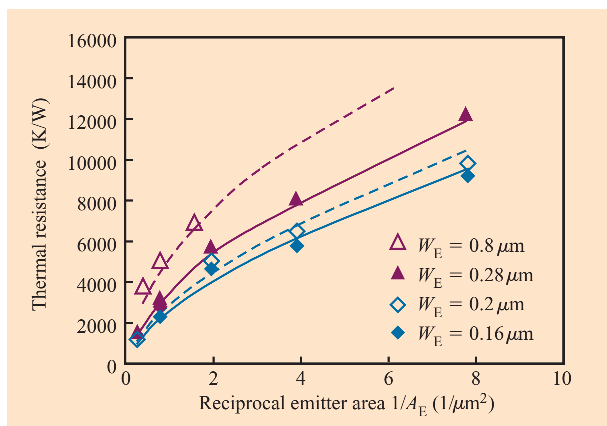

Figure 27

Measured thermal resistance for various device dimensions (symbols) for different emitter widths (W_E). The calculated thermal resistances are compared on the basis of the analytical model developed (curves). Reproduced with permission from [7]; © 2001 IEEE.

Although a variety of isolating structures are available to the designer, not all are equally effective at achieving isolation. **Figure 26** plots the additional isolation conveyed by a given strategy vs. frequency for several isolation options. Injection is considered from above the substrate (M1 to M1) and from within the substrate (n+ to n+). We observe that techniques employing deep-trench are only mildly effective (~5 dB), and only at the lower frequencies (below 20 GHz). The next most effective technique is simple separation. For each 100 μm of additional spacing between circuits, isolation is improved by approximately 18 dB. When isolating signals originating above the substrate, ground planes work quite well, with an n+ subcollector plane achieving approximately 20 dB of isolation out to beyond 25 GHz. Finally, once a signal has been injected into the substrate, a substrate contact moat may be used to collect the stray carriers, creating a large 25 dB of additional isolation, also out to beyond 25 GHz.

HBT device reliability and operating issues

HBT thermal effects

The operating temperature of semiconductor devices is of great importance, since it modulates most of the device characteristics and strongly affects the time dependence of those characteristics, or long-term reliability, as well. The actual temperature inside the device under operation, called junction temperature, is generally higher than the ambient temperature because of the self-heating effect. The internal temperature rise is determined by the thermal resistance of the device when power is dissipated. Therefore, accurate estimation of the thermal resistance is critical for the correct prediction of the device performance and its degradation under thermal/electrical stress.

Thermal resistance is commonly extracted by exploiting the temperature-sensitive electrical parameters (TSEPs), the most popular of which include base–emitter voltage, V_{BE} [78, 79] and current gain, β [80, 81]. The thermal resistances of SiGe HBTs from IBM SiGe 7HP technology have been extracted utilizing V_{BE} as a TSEP [75]. **Figure 27** shows the measured thermal resistances with various emitter dimensions, plotted as a function of reciprocal emitter area as a convenient comparison of different emitter widths. As expected, the thermal resistance increases as device size shrinks (both emitter length and width), since the heat path downward to the substrate, particularly the cross-sectional area surrounded by the deep trench, decreases with device dimension. Interestingly, however, it turns out that the junction temperature rise due to self-heating decreases with reduced device size for a fixed power density level. This can be attributed to the fact that the cross section surrounded by the deep trench per emitter area is larger for smaller devices, thereby providing a wider heat path for a given current density.

An accurate modeling of the thermal resistance would provide a reliable prediction of the thermal behavior of devices with arbitrary structural dimensions. The thermal resistance of deep-trench-isolated bipolar transistors has been modeled assuming a 45°-cone-shaped heat flow to the substrate [75]; this model exhibits an excellent agreement with measurement data for a wide range of

emitter width and length (Figure 27). The model suggests that the thermal resistance depends strongly on the geometry of the deep trench, and a substantial decrease in thermal resistance is expected when the deep-trench depth is reduced and the space between the emitter finger and the deep trench is increased.

HBT safe operation area

The bias condition of a transistor is often chosen so as to optimize the device performance for a given application. However, there exists a boundary for bias points beyond which the device may experience a serious performance drop or electrical and/or thermal instability. Since these may lead to a catastrophic device failure or device lifetime reduction as well as the malfunction of the device, it is recommended that the device be operated within such a boundary, in the safe operation area. The boundary is usually composed as a combination of two different operation limits: the voltage operation limit and the current operation limit.

The voltage operation limit is generally dictated by the avalanche multiplication process within the device and thus can be represented by the avalanche breakdown voltages. Historically, BV_{CEO} (base–open-collector-to-emitter breakdown voltage) has been widely perceived as a universal voltage limit beyond which bipolar transistors are inoperative. However, the voltage limit of a device cannot be represented by a single parameter because its avalanche behavior depends strongly on the external bias configurations and bias levels. In fact, BV_{CEO} represents just one of those cases which happens to be the worst, as is clear in the following brief review of the voltage limits given for a few widely employed bias configurations. The common emitter forced-V_{BE} configuration, dominantly found in practical bipolar circuits, exhibits a collector-to-emitter breakdown voltage that is generally larger than BV_{CEO}, since the positive feedback to the avalanche multiplication is reduced compared to the open-base situation for which BV_{CEO} is defined. The actual breakdown for this configuration is determined by the effective external resistance seen from the base as it modulates the strength of the positive feedback. Another frequently employed bias configuration is the common base forced-I_E case. For this type of configuration, the collector-to-emitter breakdown voltage is virtually identical to BV_{CBO} (emitter–open-collector-to-base breakdown voltage) because of the complete suppression of the positive feedback due to the firmly fixed emitter current level. It has been observed, however, that a lateral current instability stemming from the "pinch-in" effect [82] may result in lowered voltage operation limits. The common emitter forced-I_B configuration is rarely found in practical circuit applications, although transistor I–V characteristics are routinely plotted with this configuration. The voltage limit with this configuration is smallest and falls roughly around BV_{CEO}, with slight variation over the actual base current level. This confirms that BV_{CEO} represents the worst case of the voltage limit and bears only minor practical importance.

The current operation limit of the SiGe HBTs is determined primarily by the electromigration effect of metal lines and/or vias connected to the devices, since the device reliability is closely related to this effect (see the next section for details). With the electromigration as a limiting factor, the maximum allowed current is given as an exponential function of the temperature, making it highly sensitive to temperature variations (for example, 5°C change leads to ~35% change in the current limit). Hence, accurate temperature information at the metal interconnects becomes critical for the current limit estimation, causing the self-heating effect crucial for this purpose. Considering the power dissipation dependence of the junction temperature rise from self-heating, it is appropriate to express the current limit as a function of the device bias condition. The bias-dependent current limit has been calculated for SiGe HBTs from 7HP technology with various emitter lengths and ambient temperature of 85°C. The limit decreases with increasing voltage applied (larger power dissipation) and with increasing emitter length (larger thermal resistance). The current limit can be relaxed significantly with modified metal interconnect schemes. Also note that the limit depends on assumed values for chip lifetime, number of metal lines per chip, signal duty cycle, etc. Further relaxation of the limit can be achieved with a new set of these assumptions.

HBT reliability

The only structural difference of SiGe HBTs from conventional epitaxial-base Si bipolar transistors is the addition of a small amount of Ge in the base region. In terms of reliability, this implies that a SiGe HBT should be perceived as an extension of a Si bipolar transistor except for any effect of Ge on the reliability, if such an effect exists. After three generations of production-qualified IBM SiGe BiCMOS technology, with Ge composition now reaching 25%, we have not identified any reliability issue that can be directed to the addition of Ge. This is consistent with the observation from a similar non-IBM SiGe technology [83]. Instead, considerable suppression of boron out-diffusion from the base layer with the addition of Ge has been observed, which would result in the improvement of the base width control and stability. Therefore, it is legitimate to say that SiGe HBTs inherit the advantages of Si bipolar transistors over HBTs based on III–V systems in terms of reliability, such as minimal exposed surface area with planar structure, better

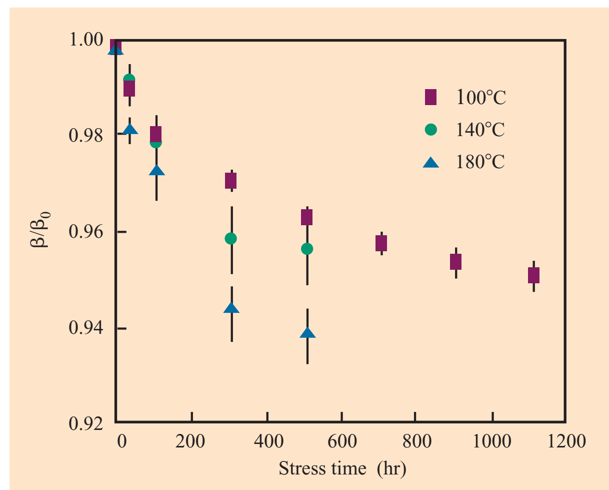

Figure 28

Typical HBT current gain degradation pattern with forward bias stress. The current density is 1.3 mA/μm^2 (near peak f_T) with device size of A_E = 0.5 μm × 2.5 μm. Reproduced with permission from [44]; © 2001 IEEE.

surface control with oxidation, and stable metal contact with silicidation, all contributing to a better reliability. The relatively high current density of SiGe HBTs, which results from the efforts to improve the operation speed, is occasionally brought up as a potential reliability issue. However, this concern comes from experience with III–V systems, in which current densities have historically been a reliability issue. Dopant diffusion in silicon systems is significantly lower than in III–V systems at operating conditions due to the highly stable Si bonding. For example, base dopant diffusion coefficients in Si are approximately 18 orders of magnitude lower than in InP systems at device operating temperatures. Thus, the effect of high current density on dopant diffusion is not a serious concern for Si systems, in contrast to III–V systems.

Typical degradation of the SiGe HBT with forward-bias long-term stress can be characterized as a gradual roll-off of the current gain, as illustrated in **Figure 28**. The degradation in the current gain usually exhibits saturation at less than ~10% with nominal operating temperatures and bias conditions, and no catastrophic failure is normally observed. The change in the current gain is attributed to electromigration-induced pressure on the emitter contact [5, 72], which is consistent with the observation from conventional Si bipolar transistors [74]. The electromigration effect does not belong to the intrinsic characteristics of the device and can be alleviated with the modification of structural and material properties of the metal interconnect.

FET device reliability and operating issues

It has been shown [84] that the reliability of FET devices in SiGe integrated technologies is comparable to that of the base technology for the major reliability mechanisms of hot-carrier, gate dielectric, and negative bias temperature instability (NBTI). The reliability models generated for the base technologies will adequately predict integrated SiGe parameter shifts and estimated lifetimes. In this section we present the major FET reliability concerns that must be addressed for analog and rf CMOS applications.

Implications of analog and rf operating point for hot-carrier degradation

The operating conditions imposed by analog and rf CMOS applications require careful attention to the reliability implications of the gate voltage (V_g) biasing point. The V_g at which we measure the drain current I_D introduces a significant source of variation on the observed level of degradation; this greatly influences the lifetime projected to achieve a given percentage of degradation. The percentage of the reduction in I_D changes drastically across the V_g value selected for the measurement. This can result in a drastic reduction in the projected lifetime of a device. Normalizing for a nominal power-supply voltage of 1.8 V, we observe a two-order-of-magnitude reduction in lifetime for a gate voltage operating point of 0.6 V—a reasonable operating point in analog circuits. Thus, using I_D at the nominal power-supply voltage as a metric for hot-carrier damage, as is often done in the case of high-speed logic, will yield overly optimistic estimates and should be carefully reviewed for adequacy with the intended circuit application and device operating conditions.

NBTI

NBTI [85] is a p-MOSFET wearout mechanism that results in a positive charge buildup and interface state generation at the Si/SiO_2 interface under the influence of applied low negative gate voltage. This mechanism exhibits a strong temperature dependence and will very likely be the dominant degradation mechanism during burn-in. It also exhibits a strong electric field dependence and will play an increasingly important role as oxides are made thinner (E_{OX} < 6.0 MV/cm; this electric field strength is lower than the field for Fowler–Nordheim injection). This mechanism has traditionally been observed with no directly measurable gate currents.

NBTI competes with channel hot-carrier damage to p-MOSFET degradation during circuit operations in advanced CMOS technologies. However, as NBTI is strongly dependent on temperature and gate bias, while hot-carrier degradation is most sensitive to channel length, hot-carrier and NBTI contributions can be separated by stressing at different temperatures.

Electromigration

Electromigration is the biased atom diffusion in interconnects during electrical current loading [86]. This redistribution of material can induce voiding near the cathodic end of interconnects, which results in a resistance increase, or even an electrical open, in circuits. Therefore, this phenomenon imposes a major reliability concern in IC operation. In particular, electromigration plays a critical role in determining the current operation limit, and thus the performance (Figure 2), of HBT devices in their high-current applications. Self-heating of HBTs at high current densities enhances the electromigration degradation [75].

Owing to stringent reliability requirements, the traditional Al(Cu) metallurgy used in BiCMOS 5/6 generations is no longer suitable for more advanced HBT circuits. Starting with the BiCMOS 7HP technology, Cu interconnects have been introduced for better electrical performance and significantly improved electromigration reliability [87–89]. As clearly demonstrated in [87] and [88], Cu interconnects offer up to ~1000× improvement in electromigration lifetime over that of traditional Al(Cu) interconnects at various elevated temperatures.

Experimentally, the electromigration current limit is determined from accelerated tests using high dc current at elevated temperatures. On the basis of the test results, the dc current limit allowed for reliable operation under use conditions can then be projected, with the acceleration factor described by

$$\textit{Acceleration factor} = \left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^{n} \exp\left[\left(\frac{\Delta H}{k}\right)\left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}}\right)\right], \tag{3}$$

where j_{stress} and j_{use} are current densities under stress and use conditions, respectively; n is the current exponent; ΔH is the activation energy associated with metal diffusion; and T_{stress} and T_{use} are respectively the interconnect temperatures under stress and use conditions. As suggested in the equation above, the electromigration current limit is very sensitive to the interconnect temperature, dictated by the activation energy ΔH; reported ΔH and n values are 0.9 eV and 1.1 for Cu and 0.85 eV and 1.7 for Al(Cu), respectively [86, 88]. The allowable current limits increase with decreasing temperature in both cases; however, Cu benefits much more significantly from a reduced temperature. Therefore, it is crucial to know the interconnect temperature under operating condition when designing for high-current applications at both the circuit and device levels.

5. Summary

These SiGe BiCMOS technologies developed at IBM use the same thorough process module development and qualification applied to previous silicon bipolar and current CMOS mainframe and server technologies. A rigorous mixed-signal application-oriented development methodology was followed in order to ensure that the correct circuit components (and with only the complexity required) were developed at each technology node and for each derivative technology. The technologies provide high-performance SiGe heterojunction bipolar transistors combined with advanced CMOS technology and a variety of passive devices critical for realizing an integrated mixed-signal system-on-a-chip. The IBM rf CMOS offerings can best be thought of as derivatives of SiGe BiCMOS. The technologies have been utilized by internal and external customers through our foundry SiGe/rf CMOS offerings to produce ICs in a wide-ranging variety of applications from 200 MHz to 50 GHz and above.

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James S. Dunn *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (jsdunn@us.ibm.com).* Dr. Dunn is a Senior Technology Staff Member in the IBM Microelectronics Division, Essex Junction, Vermont. He received the B.S., M.E. and Ph.D. degrees in materials science and engineering from the University of Utah in 1983, 1989, and 1989, respectively. In 1989 he joined IBM in Essex Junction, where he worked on BiCMOS technology development. Since 1992 Dr. Dunn has managed groups developing conventional silicon- and SiGe-based BiCMOS technologies. He holds 16 patents and has coauthored 13 papers.

David C. Ahlgren *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (ahlgren@us.ibm.com).* Dr. Ahlgren received his B.A. degree from DePauw University in 1973 and his Ph.D. degree in chemical physics from the University of Michigan in 1979. He joined IBM in Hopewell Junction, New York, in 1979 conducting semiconductor process development. His early work was in the area of silicon defects resulting from ion implantation and isolation stress, as well as process integration issues which led to the development and subsequent production of the first IBM double polysilicon bipolar technology in 1983. In 1989 his attention turned to Si/SiGe HBTs as the next step in the advancement of IBM bipolar mainframe semiconductor technology. His early device studies, process technology work, and semiconductor production experience led him into his role in the Advanced Semiconductor Technology Center as a Senior Engineer in device and process development of high-performance Si/SiGe BiCMOS technology and its introduction into manufacturing. Dr. Ahlgren is currently Senior Engineering Manager of SiGe Advanced BiCMOS Technology Development. He has published more than 30 technical papers and holds eight patents in semiconductor device and process technology.

Douglas D. Coolbaugh *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (dcool@us.ibm.com).* Dr. Coolbaugh works at the IBM Burlington, Vermont, facility in SiGe BiCMOS technology development. He is currently the technical team leader for passives development.

Natalie B. Feilchenfeld *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (feilchen@us.ibm.com).* Dr. Feilchenfeld is a Senior Scientist in the BiCMOS Technology Development Department at the IBM Essex Junction, Vermont, facility. She received an A.B. degree in chemistry from Bryn Mawr College in 1979, and M.S. and Ph.D. degrees in chemistry from Carnegie Mellon University in 1982 and 1983, respectively. After a postdoctoral appointment at the University of Chicago, she joined IBM at the Endicott Packaging Development Laboratory. She worked on photolithography and on developing new electronic plastic packages. In 1996, Dr. Feilchenfeld joined the Silicon Germanium Technology Development Group in Essex Junction, Vermont, where she and her team have been responsible for the development and qualification of low-complexity SiGe technologies (SiGe5MR, 5HPE, and 7WL). She is an author or coauthor of 12 patents and 22 technical papers. Dr. Feilchenfeld is a member of the American Chemical Society.

Greg Freeman *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (freemang@us.ibm.com).* Dr. Freeman received his Ph.D. degree in electrical engineering from Stanford University in 1991, and has since worked in the IBM Microelectronics Division. He is currently a Senior Engineering Manager, managing a department with responsibility for high-performance SiGe and rf CMOS device design, rf characterization, and compact modeling. His research interests are in the field of rf device optimization and applications. Dr. Freeman is an author or coauthor of four patents and more than 50 technical papers. He is a Senior Member of the Institute of Electrical and Electronics Engineers.

David R. Greenberg *IBM Research Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (drgreen@us.ibm.com).* Dr. Greenberg is a semiconductor device researcher working in advanced rf technology development and assessment. He received a B.S. degree in electrical engineering at Columbia University under a Pulitzer scholarship in 1988 and completed both his M.S. and Ph.D. degrees at M.I.T under Hertz and Intel Foundation fellowships in 1990 and 1994, respectively. In 1995 Dr. Greenberg joined IBM, where he has played key roles in the development of five generations of SiGe rf technology, including device design and evaluation, power transistor development, and interfacing with customer technology and circuit design groups. Most recently, he has become involved in rf CMOS technology definition. Dr. Greenberg is an author or coauthor of three patents and more than 30 technical papers. He is a member of Tau Beta Pi and the Institute of Electrical and Electronics Engineers.

Robert A. Groves *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (grovesr@us.ibm.com).* Mr. Groves received a B.S.E.E. degree from the State University of New York in 1996. He joined the IBM Corporation at the East Fishkill facility in 1989 as a Development Laboratory Technician. Since 1994, he has worked on SiGe technology development, with an emphasis on high-frequency modeling and characterization. His current focus is on interconnections, capacitors, and inductors (particularly integrated spiral inductor optimization and modeling) for microwave integrated circuits.

Fernando J. Guarín *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (guarinf@us.ibm.com).* Dr. Guarín is a Senior Engineer/Scientist at the IBM Microelectronics Semiconductor Research Development Center in East Fishkill, New York. He received a B.S.E.E. degree from the Pontificia Universidad Javeriana, Bogotá, Colombia, an M.S.E.E. degree from the University of Arizona, and a Ph.D. in electrical engineering from Columbia University. From 1980 to 1988 he was a member of the Military and Aerospace Operations Division of National Semiconductor Corporation, where he held positions in both engineering and management. In 1988 he joined the IBM Microelectronics Division, where he has worked in the reliability physics of advanced bipolar, CMOS, and SiGe technologies. Dr. Guarín holds five patents and has published more than 30 papers. He is a Senior Member of the Institute of Electrical and Electronics Engineers.

Youssef Hammad *(no biography available)*

Alvin J. Joseph *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (josepha@us.ibm.com).* Dr. Joseph received the B.E. degree in electrical engineering from Bangalore University, India, in 1989 and the M.S. and Ph.D. degrees, both in electrical engineering, from Auburn University in 1992 and 1997, respectively. His doctoral research involved the study of physics, optimization, and modeling of cryogenically operated SiGe HBTs. In 1997, he joined the IBM Microelectronics Division in Essex Junction, Vermont. He has been involved in integration and device design aspects of several generations of SiGe BiCMOS technologies. Dr. Joseph was the lead technologist/process integrator for the IBM 0.18-μm 120-GHz SiGe BiCMOS technology for production. He is a Senior Engineer and manages the SiGe technology development group responsible for installing high-speed SiGe BiCMOS technologies for production. Dr. Joseph has authored and co-authored several technical journal papers and conference publications related to SiGe devices and technologies. He has been a member of the device physics subcommittee for the IEEE Bipolar/BiCMOS Circuits and Technology Meeting and is currently serving the process technology subcommittee in the IEEE Bipolar/BiCMOS Circuits and Technology Meeting. Dr. Joseph is a Senior Member of the IEEE.

Louis D. Lanzerotti *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (lanzerot@us.ibm.com).* Dr. Lanzerotti is a Process and Device Engineer with the SiGe Technology Development Team in Essex Junction, Vermont. He received his B.S. degree in applied and engineering physics from Cornell University and his Ph.D. degree in electrical engineering from Princeton University.

Stephen A. St.Onge *IBM Microelectronics Division, Burlington facility, 1000 River Street, Essex Junction, Vermont 05452 (sstonge@us.ibm.com).* Mr. St.Onge is currently Manager of the Mixed Signal Technology Development Department at the IBM Microelectronics manufacturing facility in Essex Junction, Vermont. He has worked at that location since 1982, focusing on bipolar, BiCMOS, and SiGe BiCMOS technology development. He received a B.S. degree in electrical engineering from the University of Vermont in 1992. Mr. St.Onge is an author or coauthor of 13 patents and several technical papers. He is a member of the IEEE.

Bradley A. Orner *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (ornerb@us.ibm.com).* Dr. Orner is an Advisory Engineer in the SiGe BiCMOS Technology Development Department. He received a B.S. degree in electrical engineering from Johns Hopkins University in 1989, an M.S. degree in electrical engineering in 1995, and a Ph.D. in electrical engineering in 1997, both from the University of Delaware. Dr. Orner subsequently joined IBM at the Semiconductor Research and Development Center in Essex Junction, Vermont.

Jae-Sung Rieh *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (jsrieh@us.ibm.com).* Dr. Rieh is an Advisory Engineer in the Early Technology Definition and Evaluation Department at the IBM Microelectronics Division facility in Hopewell Junction, New York. He received B.S. and M.S. degrees in electronics engineering from Seoul National University, Korea, in 1991 and 1995, respectively, and a Ph.D. degree in electrical engineering from the University of Michigan in 1999. His doctoral research involved the development of SiGe-based electrical and optical devices and their application to microwave and optoelectronic integrated circuits. In 1999, Dr. Rieh joined the IBM Microelectronics Division in Essex Junction, Vermont, as a characterization engineer. Since 2000, he has been with IBM Semiconductor Research and Development Center, Hopewell Junction, New York, where he is involved in the design and characterization of high-speed SiGe HBTs for analog and mixed-signal applications and the analysis and modeling of the thermal and avalanche behavior of SiGe HBTs.

Kenneth J. Stein *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (kenstein@us.ibm.com).* Mr. Stein is an Advisory Engineer in the Silicon Germanium BiCMOS Department in East Fishkill. He received B.S. degrees in paper science engineering from SUNY ESF and chemical engineering from Syracuse University in 1982 and 1983, respectively. After two years at Fairchild Semiconductor, he joined IBM at the Thomas J. Watson Research Center, Yorktown Heights, New York, where he worked in the Advanced Silicon Technology facility, holding both process development and management positions. Since 1993, Mr. Stein has worked in the Semiconductor Research Development Center, first in MUV lithography and, for the past eight years, on the Silicon Germanium BiCMOS Development team, with responsibilities in the areas of FEOL, BEOL, and passives process integration. Mr. Stein holds a number of patents in the areas of capacitor and inductor fabrication.

Steven H. Voldman *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (a108501@us.ibm.com).* Dr. Voldman is a member of the Silicon Germanium Development team at the IBM manufacturing facility in Essex Junction, Vermont. He received a B.S. degree in engineering science from the University of Buffalo in 1979; an M.S. degree in electrical engineering and an E.E. degree from the Massachusetts Institute of Technology in 1981 and 1982; and an M.S. degree in engineering physics and a Ph.D. degree in electrical engineering from the University of Vermont in 1986 and 1991, respectively. In 1982, he joined IBM, working on alpha-particle effects on bipolar SRAMs; he was a member of the IBM 4-Mb DRAM, 16-Mb DRAM, CMOS logic, SOI, and SiGe technology teams. He is an author of more than 100 U.S. issued patents and 100 technical papers. Dr. Voldman is an Institute of Electrical and Electronics Engineers (IEEE) Fellow for his contributions to electrostatic discharge (ESD) in CMOS, SOI, and silicon germanium technologies.

Ping-Chuan Wang *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (pcwang@us.ibm.com).* Dr. Wang is an Advisory Scientist/Engineer in the Technology Reliability Engineering Department, where his work involves the fundamental study and modeling of reliability in electronic thin-film materials and devices. He received his doctoral degree in materials

science from Columbia University in 1997 under an IBM Cooperative Fellowship. After an appointment as a Visiting Scientist at Lehigh University, Dr. Wang joined the IBM Microelectronics Division in 1997. His current research interests include the development and application of a synchrotron-based X-ray microbeam system to study material properties in micron scale. Dr. Wang is an author or co-author of more than 30 technical papers and one U.S. patent.

Michael J. Zierak *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (zierakm@us.ibm.com).* Dr. Zierak received B.S., M.S., and Ph.D. degrees in electrical engineering from Rensselaer Polytechnic Institute in 1991, 1992, and 1997, respectively. His doctoral studies involved InGaAs and InGaAsSb material engineering and device design for thermophotovoltaic power generation. Since joining IBM in 1997, he has worked on process integration and device design in SiGe BiCMOS technologies. Dr. Zierak is currently an Advisory Engineer in the SiGe Technology Development Department.

Seshadri Subbanna *IBM Systems Group, 2455 South Road, Poughkeepsie, New York 12601 (subbanna@us.ibm.com).* Dr. Subbanna received his B. Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, and his M.S.E.E. degree and Ph.D. degree in electrical engineering and materials science from the University of California at Santa Barbara. His doctoral work was on optical and electronic properties of antimonide superlattices and heterostructures, including the first observation of quadratic piezo-electro-optic effect in strained superlattices. From 1989 to 2002, Dr. Subbanna was with the IBM Microelectronics Division in East Fishkill, New York. Since joining IBM, he has worked on advanced bipolar and CMOS processes, high-density SRAM development, and BiCMOS technology. From 1996 to 2002, he was manager of advanced silicon–germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS development at the IBM Microelectronics Semiconductor Research and Development Center in East Fishkill. This group was the first to achieve over 200 GHz high-frequency performance in a silicon-based technology, and it is recognized worldwide as a leader in the development of high-speed networking technology. He was also a senior business counsel charged with intellectual property development and patent generation. Currently Dr. Subbanna is on assignment with the IBM Systems Group (previously the IBM Server Group). He has given many invited talks, and has over 50 publications and 20 patents to his credit.

David L. Harame *IBM Microelectronics Division, Burlington facility, 1000 River Road, Essex Junction, Vermont 05452 (dharame@us.ibm.com).* Dr. Harame received a B.A. degree in zoology from the University of California at Berkeley in 1971 and an M.S. degree in zoology from Duke University in 1973. He also received an M.S. degree in electrical engineering from San Jose State University in 1976 and an M.S. degree in materials science and a Ph.D. in electrical engineering, both from Stanford University in 1984. He then joined the IBM bipolar technology group at the IBM Thomas J. Watson Research Center, where he worked on the fabrication and modeling of Si-based integrated circuits. His research interests at Yorktown Heights included Si transistors, SiGe-channel FET transistors, npn and pnp SiGe-base bipolar transistors, complementary bipolar technology, and BiCMOS technology for digital and analog and mixed-signal applications. In 1993 he joined the IBM Semiconductor Research and Development Center in the Advanced Semiconductor Technology Center (ASTC) in Hopewell Junction, New York, where he was responsible for the development of SiGe technology for mixed-signal applications. He managed SiGe BiCMOS technology development at the ASTC through 1997. In 1998 Dr. Harame joined the IBM manufacturing organization in Essex Junction, Vermont, where he managed a SiGe technology group and the installation of the 0.5-mm SiGe BiCMOS process into manufacturing. In 1999 he co-managed the qualification of a 0.25-μm SiGe BiCMOS as well as 0.18-μm SiGe BiCMOS and two derivative SiGe BiCMOS technologies. In 2000, he became the Senior Manager of the RF Analog Modeling and Design Kit Department. Dr. Harame is a Distinguished Engineer of the IBM Corporation, a Senior Member of the IEEE, an Executive Committee member of the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), and a member of the Compact Model Council.

Dean A. Herman, Jr. *IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (dean@us.ibm.com).* Dr. Herman is Manager of Analog and Mixed Signal Operations, Office of the Chief Technologist, IBM Technology Group. Until recently he managed the groups doing research and development on the IBM SiGe technologies and on the design kits for all IBM analog and mixed-signal technologies; this effort included the IBM high-frequency measurement and modeling efforts. Dr. Herman received a B.S. degree in engineering from the U.S. Military Academy at West Point, New York, in 1960, and M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1967 and 1975, respectively. He taught in the Department of Electrical Engineering at West Point for 15 years and was Professor and Deputy Head of the Department prior to joining IBM in 1986. He is a Senior Member of the Institute of Electrical and Electronics Engineers.

Bernard S. Meyerson *IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (meyerson@us.ibm.com).* Dr. Meyerson is Chief Technologist, IBM Technology Group, also serving as Vice President, IBM Communication Research and Development Center. He received a Ph.D. degree in solid-state physics from the City College of the City University of New York in 1980 and subsequently joined IBM at the Thomas J. Watson Research Center to work on the chemical fundamentals of electronic materials thin-film deposition. His work led to the development of ultrahigh-vacuum/chemical vapor deposition (UHV/CVD), a technique which proved successful for the epitaxial deposition of a wide variety of Si-based alloys under conditions, and having chemical compositions which lay well outside accepted bounds on such processes and materials. Most significant was the deposition of production quantities of SiGe epitaxial layers at temperatures of 500°C and below, resulting in the development of extremely high-performance SiGe heterjunction bipolar transistors (HBTs). Under his leadership, a complete SiGe HBT technology was developed, demonstrating high levels of integration at performance characteristics representing a discontinuity in historical trends for bipolar technology. Although the technology was initially intended for computing applications, Dr. Meyerson refocused it into a communication-centric technology. By 1992, he had launched a series of now well-publicized IBM alliances to leverage this technology trend, over the years incorporating organizations as diverse as Alcatel, Analog Devices, Hughes, Harris Semiconductor (now Intersil), Leica, National

Semiconductor, Nortel, Tektronix, and many others. Early adoption of the technology has led to numerous commercial and consumer products, 40-Gb/s SONET standard data systems and 802.11b 11-Mb/s wireless LAN cards being limited examples. IBM's lead into this marketplace has resulted in general technology acceptance after ten years of controversy, with all major communications technology providers announcing upcoming, competing market entries. In 1998, the IBM analog and mixed-signal technology development was consolidated under Dr. Meyerson. In 2002, he became Vice President of the Communications Research and Development Center, a multinational organization encompassing IBM's worldwide communications technology and circuit design efforts and supporting a rapidly growing worldwide customer base. In 1992, Dr. Meyerson was designated as an IBM Fellow. He is also a Fellow of the American Physical Society and the IEEE. He holds more than 40 patents and has published several hundred technical papers. He has received numerous awards for his work, including the Materials Research Society Medal (1991) and the Electrochemical Society Electronics Division Award (1993); he was cited as "Inventor of the Year 1997" by the New York State Legislature and was honored as the 1999 "United States Distinguished Inventor of the Year" by the U.S. Patent and Trademark Office. He recently received the 1999 IEEE Ernst Weber Award for the body of work culminating in the commercialization of SiGe-based communications technology. In December 1999, he received the IEEE Electron Devices Society J. J. Ebers Award, and in 2002 he was inducted into the National Academy of Engineering. His team's work has been featured in a long-term ongoing study by the Lally School of Business Management, exploring the management of discontinuous innovation within large organizations.